German Jordanian University

Electronics 1 Lab (CME 2410)

School of Informatics & Computing
German Jordanian University

Laboratory Experiment (3)

Prelab:

1. Simulate the procedure describe in Part I, Section 5d (Negative Polarized Clipper).
2. Prepare a short report with simulation results.

Part I - Diode Clipper

1. Objective:

To know the behavior of clipper circuit (simple and double)

2. Theory:

Clipper Circuit:

The clipper circuits have the properties of selecting a part of the applied waveform that can be higher or lower to a reference level or included between two reference levels.

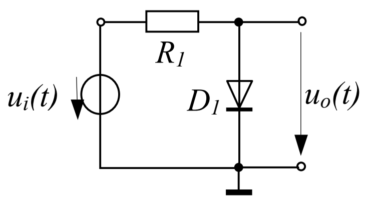


Fig. 2.1: clipper

By assuming for the diode D the characteristic of an ideal diode and for the input voltage a positive value ($u_i > 0$), the diode is forward biased and, being ideal, the output voltage u_o is equal to zero.

When, instead, the input voltage has a negative value ($u_i < 0$), the diode D is reverse biased and it doesn't conduct: the output voltage u_o is equal to the input voltage u_i.

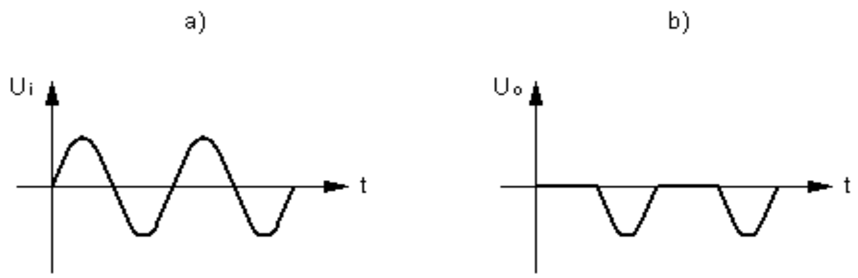


Fig. 2.2: The output (b) of a sinusoidal input voltage (a).

In practice the positive part of the signal over the zero limit has been "cut".

3. Equipment & Instruments

- Module No. : DL 3155E12
- Function Generator
- Oscilloscope

4. Components List:

R1 = 10 kΩ - 1/4W - 5%

R2 = 5 kΩ - manual regulation trimmer

R3 = 5 kΩ - manual regulation trimmer

D1 = Silicon diode - 1N4007

D2 = Silicon diode - 1N4007

Calculation data: Voltage drop at a forward biased silicon diode: $U_{threshold} \approx 0.6V$

5. Procedure

- Insert the Module 12 in the console and set the main switch to ON;

a) POSITIVE CLIPPER

3. set the switches S1 to ON and S2 to OFF and turn, completely counterclockwise, the potentiometer R2;
4. connect the signal generator and the oscilloscope as shown in Fig. 2.3-a.;
5. adjust the oscilloscope in the following way:
   CH1 and CH2 = 1 V/DIV,
   SWEEP = 1 ms/DIV,
   Coupling = DC;

6. without supplying the signal generator, superpose, at the half of the oscilloscope display, the line of channel 1 and the line of channel 2;
7. supply the signal generator and adjust the output to a sinusoidal voltage of $V_{pp} = 6$ V and f = 200 Hz;
8. observe the displayed output signal: the positive half-waves have been cut at a level that corresponds to the diode threshold (0.6V);
9. draw in Fig. 2.4-a the signals displayed on the oscilloscope.

b) NEGATIVE CLIPPER

1. set the switches S1 to OFF and S2 to ON and turn, completely counterclockwise, the potentiometer R3: the diode polarity used in the circuit is inverted;
2. connect the signal generator and the oscilloscope as shown in Fig. 2.3-b;
3. Draw in Fig. 2.4-b the output signal displayed on the oscilloscope: in this case all the negative half-waves have been removed;
4. compare the output wave of the negative clipper with the one of the positive clipper and describe the differences that have been found;

c) POSITIVE POLARIZED CLIPPER

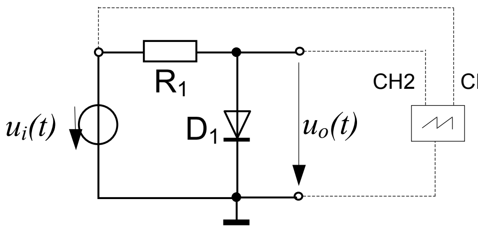
1. set the switches S1 and S2 on OFF
2. turn the potentiometer R2 in such a way to read, on the jack 3, a voltage of 1 V: use the oscilloscope to effectuate this reading;
3. set the switch S1 to ON;
4. repeat the procedure of points with the red arrow;
5. observe the displayed output signal: the positive half-waves are cut, against the positive clipper, at a higher level that corresponds to the polarization direct voltage (1 V) added to the diode threshold voltage (0.6 V);
6. draw in Fig. 2.4-c the output signal displayed on the oscilloscope;

d) NEGATIVE POLARIZED CLIPPER

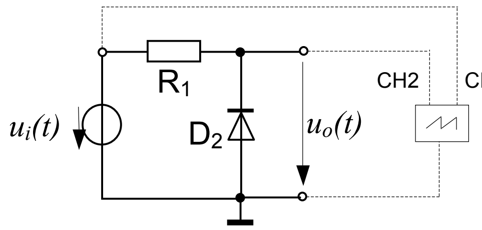
1. set the switches S1 and S2 to OFF;
2. turn the potentiometer R2 in such a way to read, on the jack 4, a voltage of -1 V: use the oscilloscope to effectuate this reading;
3. set the switch S2 to ON;
4. observe the displayed output signal to compare it to the one of the positive polarized clipper and describe the differences that have been found;
5. Draw in Fig. 2.4-d the output signal displayed on the oscilloscope.

e) <u>INDEPENDENT LEVEL DOUBLE CLIPPER</u>

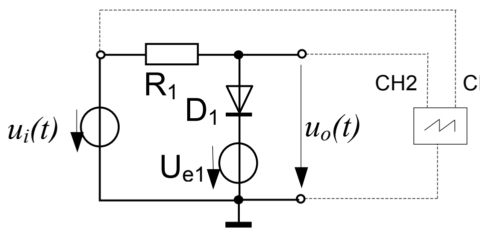
1. set the switches S1 and S2 to ON;
2. observe the displayed output signal, draw it in Fig. 2.4-e, describe the differences that have been found with the previous circuits;
3. observe what happens for the different voltage values applied to the jacks 3 and 4, by adjusting the potentiometers R2 and R3.



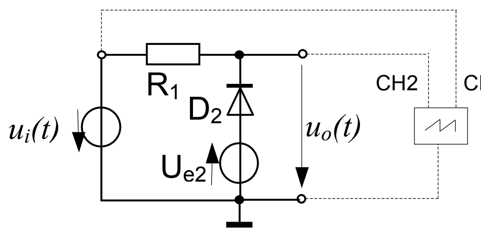
(a)



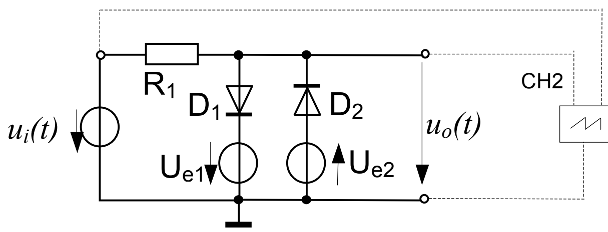
(b)



(c)



(d)



(e)

Fig. 2.3

a) positive clipper
b) negative clipper
c) positive polarized clipper
d) negative polarized clipper
e) independent level double clipper

6. Results

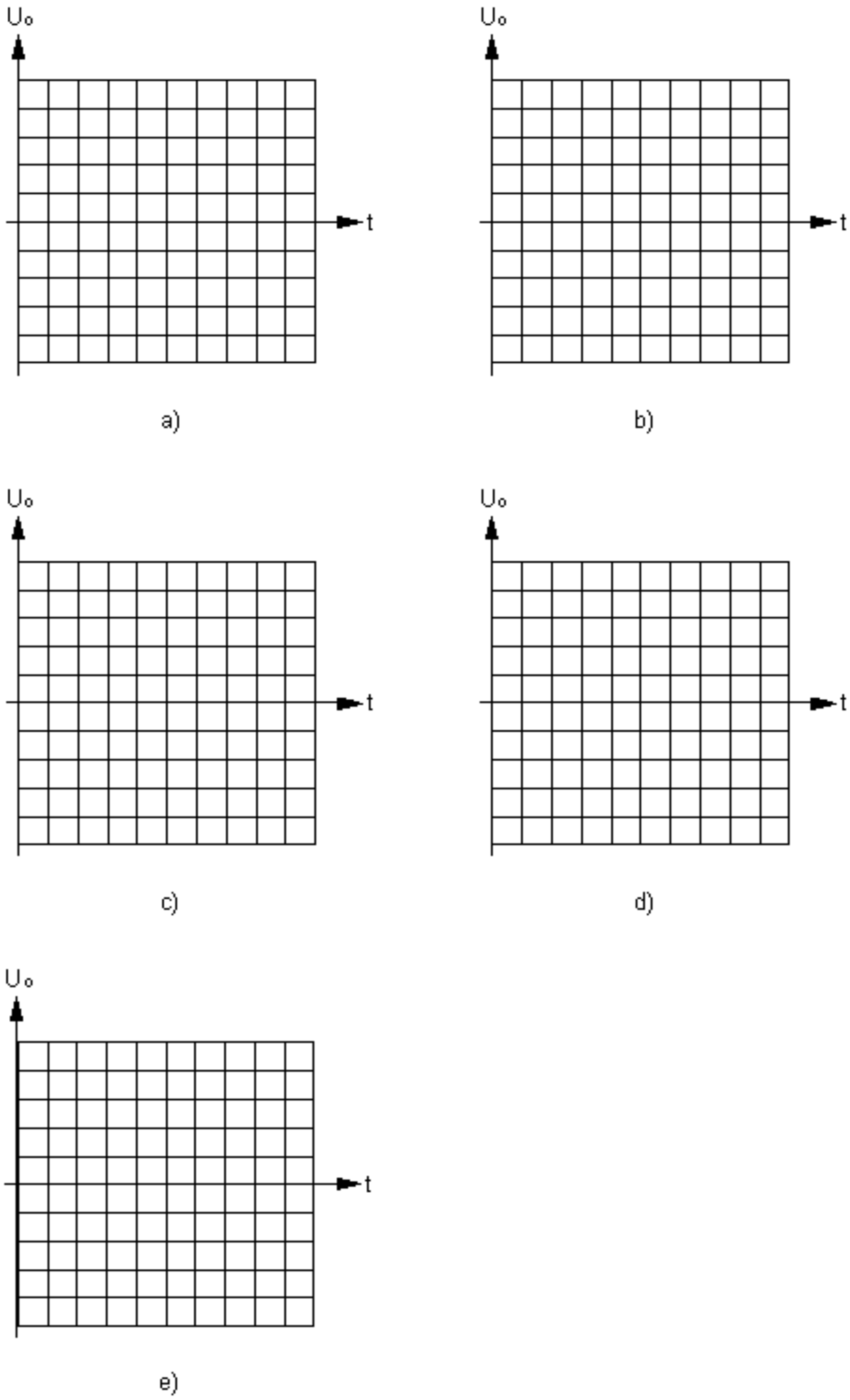


Fig. 2.4

a) positive clipper
b) negative clipper
c) positive polarized clipper
d) negative polarized clipper
e) independent level double clipper

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7. *Questions:*

A. The positive peak voltage of a positive clipper is:

1- 0 V
2- 0.6 V
3- Equal to the input peak voltage
4- 1.2 V

B. Why is the positive peak voltage in the negative clipper not cut?

1- The diode is forward biased
2- The diode is reversed biased

C. In a positive polarized clipper we found the voltage source in series to the diode equal to be +5V. Which is the cut level of the positive voltage?

1- 0.6
2- Equal to the input peak voltage
3- 5 V
4- 5.6 V

Part II - Clamper and Voltage Multiplier

1. *Objective*:

To be familiar with the clamper circuits, the voltage doubler and voltage multiplier.

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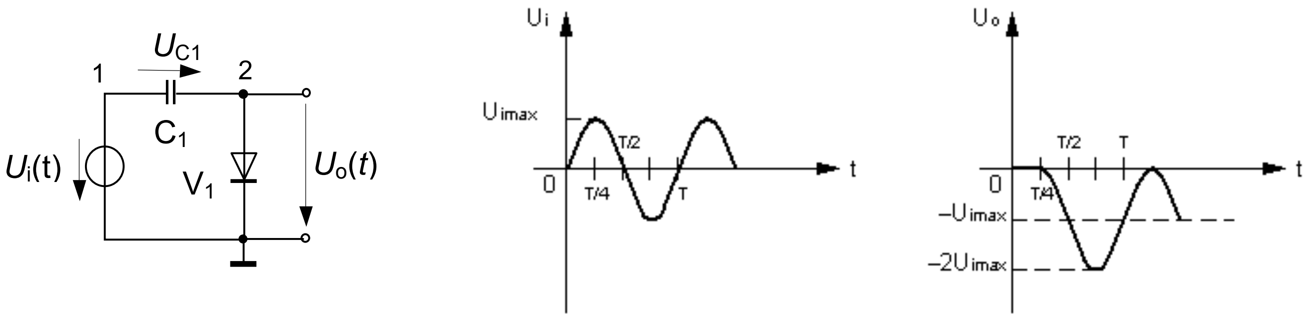
2. *Theory*:

A) CLAMPING CIRCUITS

While the clipping circuit cuts a part of the input signal, the clamping circuit adds to the signal a positive or negative DC component due to a charged capacitor.

Consider for example the circuit of the Fig. 4.1 a (negative clamper).

Let's suppose that the generator delivers an alternating voltage $U_i(t)$ (s. Fig. 4.1 b) with the peak value of $U_{i\,\max} = 10$ V and that the diode V1 is ideal (no resistance for $U_F \geq 0$ V with the threshold voltage of $U_{th} = 0$ V).



(a) (b) (c)

Fig. 4.1 Negative Clamper

Switching on $U_i(t)$ the capacitor C1 is initially uncharged ($U_{C1} = 0$ V). In the positive cycle the diode V1 conducts as points 1 as well as point 2 are positive to ground. As V1 shows (almost) no resistance the capacitor is charged instantaneously. The voltage U_{C1} equals the input voltage $U_i(t)$ until its maximum value $U_{C1} = U_{i\,\max} = +10$ V.

For $T/4 \leq t \leq T/2$ the input voltage $U_i(t)$ decreases from the maximum value +10 V. Point 2 finds itself at a negative potential to ground as the diode V1 doesn't conduct in reversed biases mode and the capacitor cannot discharge. The voltage U_{C1} is still **clamped** to its maximum value $U_{C1} = U_{i\,\max} = +10$ V.

Applying the KVL the output voltage $U_o(t)$ gets

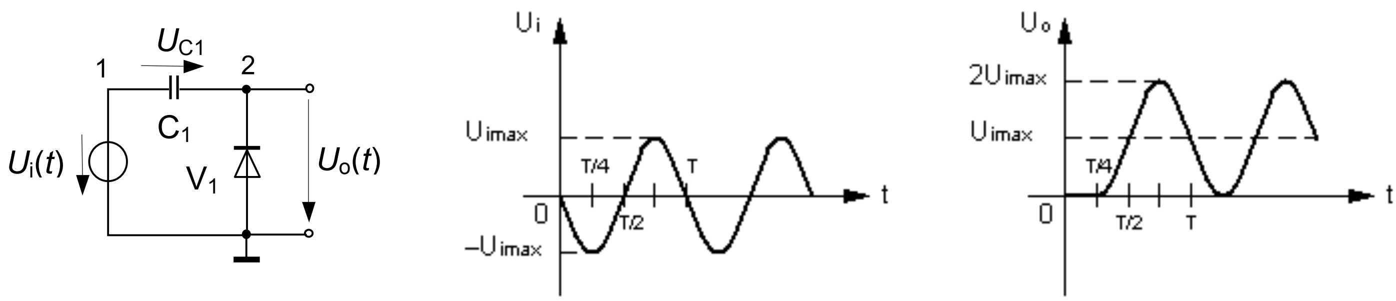
$$U_o(t) - U_i(t) + U_{C1} = 0$$
$$\Rightarrow U_o(t) = U_i(t) - U_{C1}$$

As the capacitor C1 can't discharge anymore the voltage U_{C1} is constant at the value $U_{C1} = U_{i\,\max} = +10$ V and the output voltage $U_o(t)$ is simply the alternating input voltage $U_i(t)$ shifted to the negative polarity by $U_{i\,\max} = 10$ V (s. Fig. 4.1 c):

$$U_0(t) = U_i(t) - U_{C1} = U_i(t) - U_{i\,\max} = U_i(t) - 10\ \text{V}$$

In the circuit of Fig. 4.2 (positive clamper)
the direction of the diode V1 is **opposite** to Fig. 4.1. Here the negative cycle will charge the capacitor C1 to the negative value of the alternating voltage $U_{C1} = -U_{i\,\max} = -10\ \text{V}$ and this voltage is clamped to the input value. As all reference polarities are kept unchanged we can use the same equation as above:

$$U_0(t) = U_i(t) - U_{C1} = U_i(t) - U_{i\,\max} = U_i(t) - (-10\ \text{V}) = U_i(t) + 10\ \text{V}$$



(a) (b) (c)

Fig. 4.2 Positve Clamper

With a resistive load R1 in parallel to the diode, the capacitor aims to discharge through this load. If the discharge time is sufficiently long, the voltage at the capacitor U_{C1} is not able to vary appreciably: since the discharge time is of the order of R1 · C1 it is therefore necessary that R1 · C1 >> T, where T is the period of the alternated signal.

For example for a load equal to R1 = 1000 Ohm and for frequencies in the order of f = 50 Hz it is necessary a capacitor with a capacity of $C1 \geq 100\ \mu\text{F}$.

B) VOLTAGE DOUBLER

In the circuit of Fig. 4.3 (voltage doubler) the positive clamper is followed by a half-wave rectifier (see former experiment). Although the input to the rectifier is a pulsating and not an alternating voltage (see Fig. 4.3 c) the capacitor C2 will be charged to the maximum voltage $U_{C2} = 2 \cdot U_{i\,\max}$ (see Fig. 4.3 d). In absence of a load to the capacitor C2 the output voltage will keep constant at the double value of the input voltage:

$$U_o(t) = U_{C2} = 2 \cdot U_{i\,\max}$$

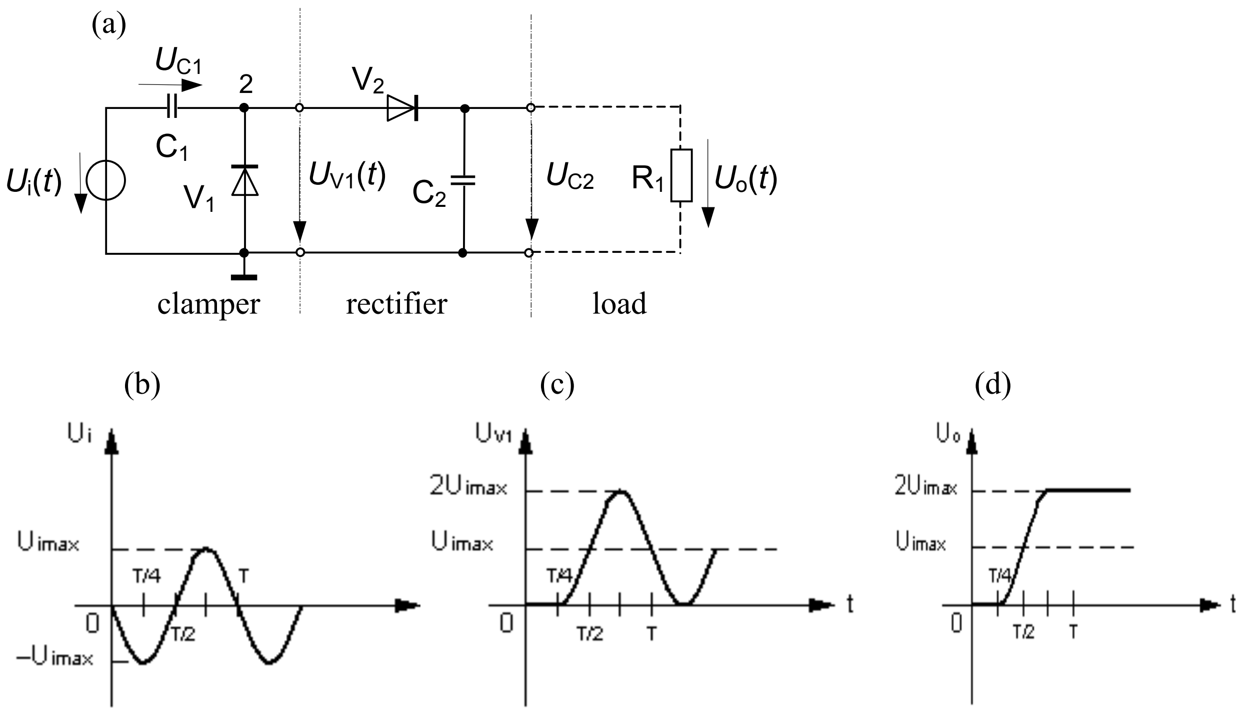


Fig. 4.3 Voltage Doubler

To determine the maximum reverse voltage $U_{\mathrm{RV1\,max}}$ of the diodes (also named Peak Inverse Voltage PIV) the KVL should be applied.

C) VOLTAGE MULTIPLIER

To get a more general understanding of adding voltages with charged capacitors and diodes we make two minor changes to the circuit of Fig. 4.2 (see Fig. 4.4):

- To get positive numerals for the clamped voltages at all capacitors the reference polarity at capacitor C1 is turned (from right to left).
- As the order of elements in one branch is arbitrary we change the order of the diode V2 and the capacitor C2;

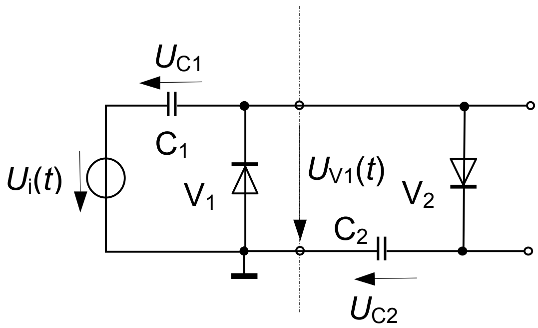


Fig. 4.4 Voltage Doubler

As discussed above the negative cycle of the input voltage $U_i(t)$ charges capacitor C1 via diode V1 and the positive cycle charges capacitor C2 via V2 while U_{C1} is constant at

$\underline{U_{C1} = U_{i\,\max}}$.

C2 is charged to

$U_{C2} = U_i(t) + U_{C1}$

or using the clamped voltages:

$\underline{U_{C2}} = U_{i\,\max} + U_{i\,\max} = \underline{2 \cdot U_{i\,\max}}$

We add another diode-capacitor section (see Fig. 4.5).
As discussed above the negative cycle of the input voltage $U_i(t)$ charges C1 via diode V1 and in addition C3 via V3. The voltage U_{C3} is easily identified by using KVL:

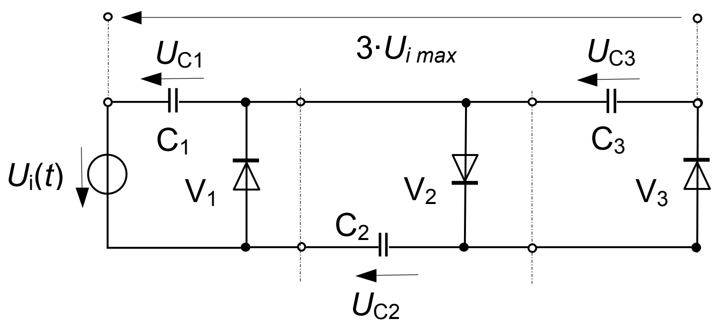


Fig. 4.5 Voltage Tripler

$$U_{C3} + U_{C1} + U_i(t) - U_{C2} = 0$$

$$U_{C3} = U_{C2} - U_{C1} - U_i(t)$$

Replaced by the clamped voltages $U_{C2} = 2 \cdot U_{i\,\max}$, $U_{C1} = U_{i\,\max}$ and $U_i\ (t) = -U_{i\,\max}$

$$U_{C3} = 2 \cdot U_{i\,\max} - U_{i\,\max} - (-U_{i\,\max})$$

$$U_{C3} = 2 \cdot U_{i\,\max}$$

A $\underline{3 \cdot U_{i\,\max}}$ output is taken across C1 and C3 (see Fig. 4.5).

Adding more diode-capacitor section (see Fig. 4.6) we get a lattice network. Every new capacitor adds a voltage of $2 \cdot U_{i\,\max}$.

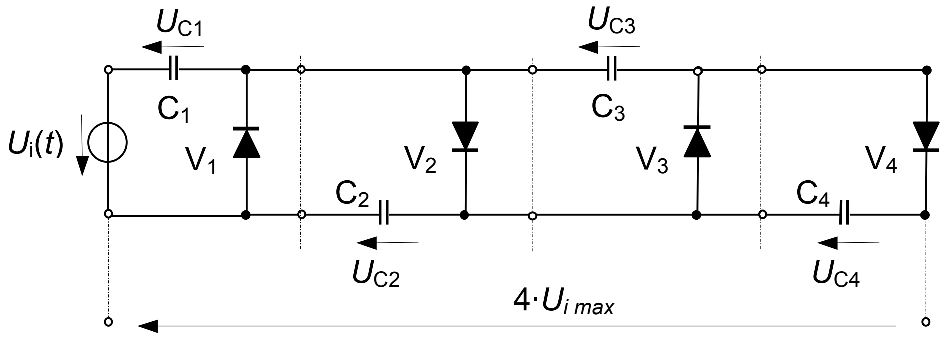


Fig. 4.6 Voltage Quadrupler

3. *Questions*:

a. The diodes are never ideal. They always have a threshold voltage.
   Calculate the maximum output voltage of the Negative Clamper with a diode of $U_{th} = 0.6\ \text{V}$.
b. Calculate the output voltage of the voltage doubler with diodes of $U_{th} = 0.6\ \text{V}$.
c. Prove for the Voltage Quadrupler that the new diode-capacitor section adds a voltage of $U_{C4} = 2 \cdot U_{i\,\max}$.
d. Calculate for the Voltage Tripler the maximum reverse voltages (or peak inverse voltages) of all diodes.
e. Compared to normal transformer name at least one advantage and one disadvantage of a Voltage Multiplier.
f. Give 3 concrete examples for the practical application of the voltage multiplier.

4. *Equipment & Instruments*:

- Module No. : DL 3155 M12
- Function Generator
- Oscilloscope
- $R1 = 10\ \text{k}\Omega\ \ (1/4\ \text{W} - 5\ \%)$

5. *Procedure*:

The negative and positive clamper

All measurements have to be made for the negative as well as for the positive clamper.

1. Use the module named above;
2. Identify how to realize the negative as well the positive clamper;
3. Connect the signal generator and the oscilloscope to your circuit.
4. Set the signal generator output to a sinusoidal voltage of about

$$U_{i\ \max} = 2\ \text{V}$$
$$f = 1\ \text{kHz}$$

5. Sketch the input and output signals displayed.
6. Vary the peak voltage and the frequency of the input voltage, observe and describe what happens.

The voltage doubler

1. Identify how to realize the voltage doubler (see Fig. 4.3 a);
2. Connect the signal generator and the oscilloscope to your circuit.
3. Set the signal generator output to a sinusoidal voltage of about

$$U_{i\ \max} = 2\ \text{V}$$
$$f = 1\ \text{kHz}$$

4. Sketch the input and output signals displayed.
5. Vary the peak voltage and the frequency of the input voltage, observe and describe what happens.