الجامعة الألمانية الأردنية
German Jordanian University

Electronics 1 Lab (CME 2410)

School of Informatics & Computing
German Jordanian University

Laboratory Experiment (10)

Junction FETs

1. *Objective*:

- the operation of a junction field-effect transistor (J-FET)
- the characteristic curves of a J-FET
- the gate bias of a J-FET

2. *Theory:*

Fundamentals

The name J-FET means Junction (one PN junction) and Field-Effect (reverse biased junction) Transistor. It is called a "unipolar" device as only the majority charge carriers are contributing to the current.

Fig. 9.1 shows the three terminals of a J-FET: gate, source and drain.

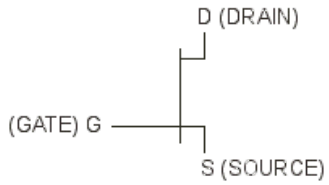

Fig. 9.1 - Three terminals of a J-FET

J-FETs are either N-channel or P-channel semiconductor devices. Fig. 9.2 shows the symbol for each type of device.

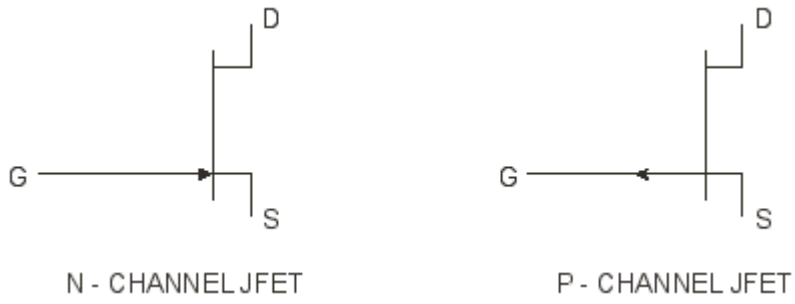

Fig. 9.2 - N- and P-channel J-FET symbols

J-FETs are depletion mode FETs. It is normally conductive between drain and source, which is called the "channel", and must be biased into its off state.

J-FETs are voltage-operated, current-controlling devices. The current is **only** flowing through the J-FET channel. The amount of this drain-source current flow is controlled by the width of the depletion region which is determined by the gate-to-source bias voltage applied to the J-FET. The drain-source current or simply drain current is the only current because there is no gate current if properly biased. There is only an extremely low current of minority charge carriers.

Fig. 9.3 shows a working model of an N-channel J-FET and its depletion region.

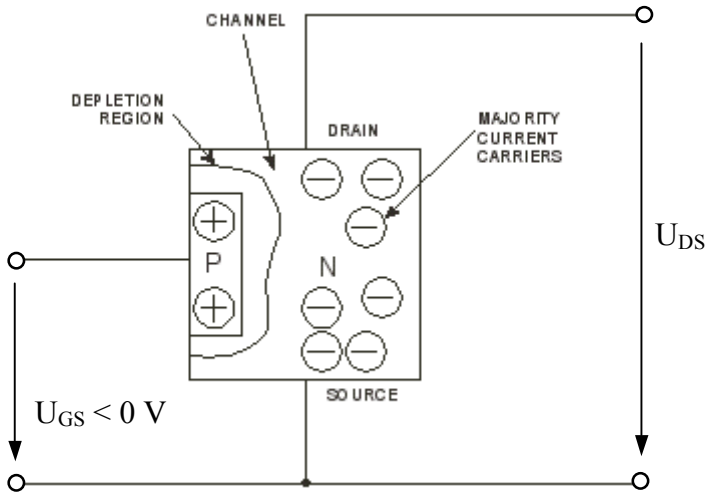

Fig. 9.3 - N-channel J-FET model

In Fig. 9.3, the PN-junction, or gate-to-channel diode, must always be reverse biased to control the channel current. With sufficient bias, channel current can be reduced to zero (device turned off).

For N-channel J-FET the width of the depletion region is increased by a more negative gate-to-source bias voltage for the P-channel J-FET the voltage has to be positive.

J-FETs have very high input impedance provided that the gate-to-source bias voltage does not forward bias the gate-to-channel PN junction.

Fig. 9.4 shows the proper bias voltages required for an N-channel and a P-channel J-FET. The figure also indicates proper U_{DS} (drain-source voltage) polarity.

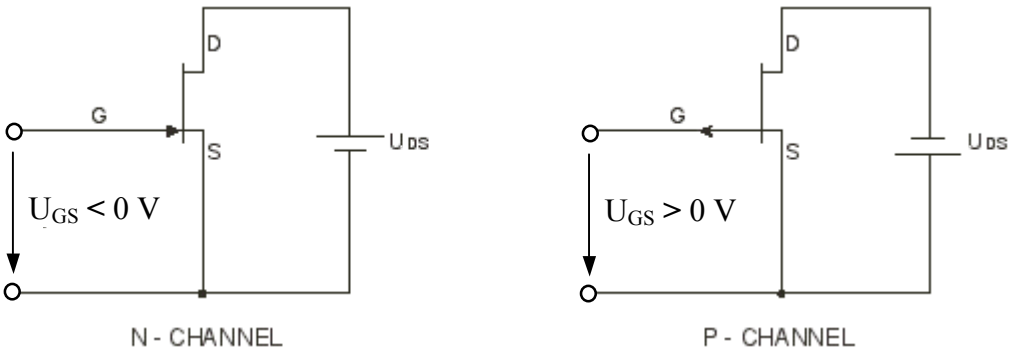

Fig. 9.4 - N-channel and P-channel bias voltages (mind different polarities!)

J-FETs are linear devices that exhibit an ohmic region (or resistive region).

On a J-FET characteristic curve, the ohmic region falls between the zero and saturation channel current points.

Fig. 9.5 illustrates a J-FET characteristic curve and its major operational points.

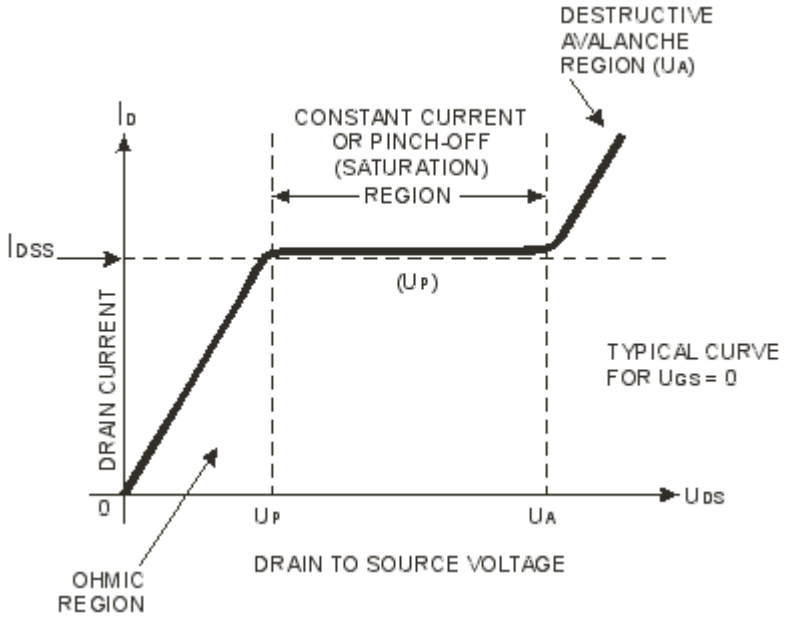

Fig. 9.5 - Typical J-FET characteristic curve

J-FETs have a natural resistance to electrostatic discharge and are not easily harmed; however, you should use caution when you handle FETs.

b) J-FET Operating characteristics

On the J-FET characteristic curve in Fig. 9.6, pinch-off (saturation region) voltage is represented by U_P. At this point, an increase in drain voltage does not increase the drain current.

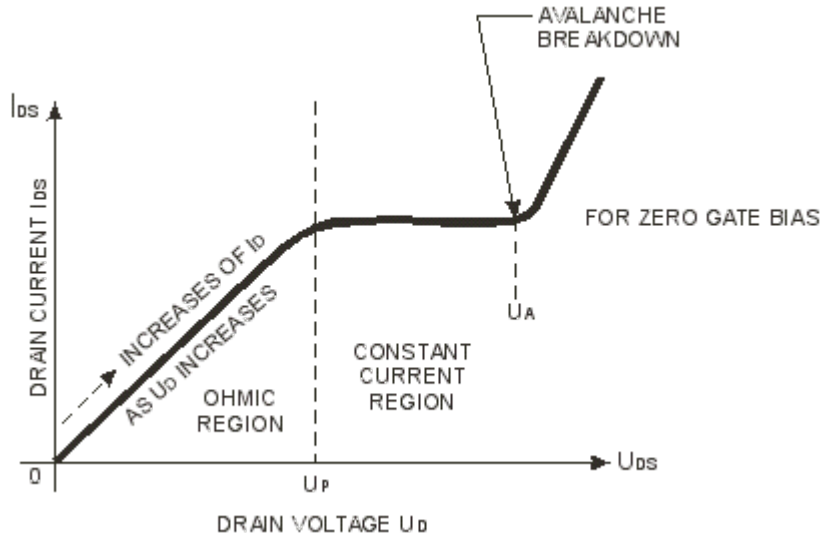

Fig. 9.6 - J-FET operating curve points

Drain current (I_D or I_{DS}) increases as drain-source voltage (U_{DS}) increases until pinch-off saturation of the J-FET device occurs.

Within the saturation range of a J-FET the drain-source current is nearly constant. For zero gate bias this drain current is referred to as I_{DSS} or $I_{DS(sat)}$.

Below the pinch-off point U_P, I_D is dependent on U_{DS}. This range of operation is the ohmic region of the J-FET.

A considerable variation exists in the U_P points of the same type of J-FETs.

Beyond the saturation point of a J-FET, increasing U_{DS} produces avalanche breakdown and will destroy the J-FET.

A J-FET operating in its ohmic region can be represented by a variable resistor.
Within the ohmic region, current flow through the J-FET varies according to Ohm's law.

c) The effect of Gate Bias on Pinch-off

The drain current of a J-FET may be reduced to zero by sufficient gate bias (in a reverse direction). This operation is referred to as cut-off.

J-FETs are operating with gates in zero or reverse biased states. Applying a forward bias to a J-FET gate allows gate current to flow which is not wanted.

A reverse biased J-FET gate does not draw gate current from the external bias circuit. The gate represents very high impedance to the external bias circuit.

For a fixed value of drain-source voltage, the operating curve of a J-FET circuit is determined by the applied gate-to-source bias voltage.

One major effect of gate bias is the reduction in the value of the pinch-off (saturation) voltage level.

J-FETs usually operate with a maximum of 5 volts of reverse bias gate voltage. Higher voltages can destroy the gate-to-channel PN junction.

An N-channel J-FET requires a negative gate voltage (with respect to the source) in order to deplete the channel. When the channel is depleted, the device turns off because the negative bias voltage has generated a large depletion area. This area effectively blocks the flow of drain current.

d) J-FET Dynamic Characteristic Curves

A J-FET can be used as an amplifier (this concept will be covered in lesson 2 of this manual).

Dynamic operating curves are used to predict performance levels of J-FETs. A family of curves requires that both the U_{DS} and U_{GS} voltages be adjustable.

(In this experiment is no measurement prepared concerning the dynamic characteristic.)

3. Equipment & Instruments

Module No. : DL 3155E18 unit
- Function Generator
- Oscilloscope

4. Components List:

R1 = 1 MΩ - ¼ W
R2 = 100 Ω - ¼ W
R3 = 100 Ω - 2 W
V1 = 2N5459
V2 = 1N4007

5. Procedure:

J-FET OPERATING CHARACTERISTICS

$I_{DS} = f(U_{DS})\big|_{U_{GS}=0}$

1) insert the Module E18 unit (1) in the console and set the main switch to ON;
2) connect the circuit as shown in Fig. 9.7a;
3) set the multimeter (1) as dc voltmeter and adjust drain-source voltage U_{DS} (with the positive variable supply) for $U_{DS} = 0.5$ V;
4) set the multimeter (2) as dc milliammeter and measure the drain-source current I_{DS} through the J-FET;
5) note all values I_{DS} when increasing U_{DS} up to 10 V in steps of $\Delta U_{DS} = 0.5$ V (name this table Tab. 9.1a)
6) plot the measured values as $I_{DS} = f(U_{DS})$ (name this graph Fig. 9.8a);
7) explain the purpose of resistor R2; is the gate zero biased?
8) mark on the plotted curve the transition point from the ohmic region to the constant current region and record the value of this voltage;
10) note that the drain-source current I_{DS} increases with drain-source voltage U_{DS} in the ohmic region of the curve;
11) note also that the drain-source current I_{DS} of a zero biased J-FET device can be reduced to zero only if the drain-source voltage U_{DS} is reduced to zero voltage;

EFFECT OF GATE BIAS ON PINCH-OFF

$I_{DS} = f(U_{GS})\Big|_{U_{DS}=const.}$

13) connect the circuit as shown in Fig. 9.7b;
14) adjust the gate-source bias supply for $U_{GS} = 0$ V;
15) adjust the drain-source supply for $U_{DS} = 10$ V;
16) measure and record the values of the drain-source current I_{DS} varying the gate-source bias from $U_{GS} = 0$ V to $U_{GS} = -2.5$ V in steps of $\Delta U_{GS} = 0.5$ V (name this table Tab. 9.1b);
17) repeat the measurement for $U_{DS} = 5$ V
18) verify, based on the results of Tab. 9.1b, that the gate bias voltage U_{GS} needed to turn off the J-FET remains about the same as the drain-source voltage U_{DS} changes;
19) verify, based on the results of Tab. 9.1b, that the pinch-off (saturation) point of the J-FET (U_P) decreases as the gate bias voltage U_{GS} increases;
20) plot the graphs $I_{DS} = f(U_{GS})$ (name this graph Fig. 9.8b);

$I_{DS} = f(U_{DS})$ for two different U_{GS}

21) adjust the gate-source bias voltage for $U_{GS} = -0.5$V;
22) measure and record the values of the drain-source current I_{DS} varying the drain-source voltage from $U_{DS} = 10$ V down to $U_{DS} = 0$ V in steps of $\Delta U_{DS} = 1$ V, acquire additional values for $U_{DS} = 0.5$ V and $U_{DS} = 0.25$ V (name this table Tab. 9.2);
23) repeat the measurement for $U_{GS} = -1.5$ V and record them in a second column of Tab. 9.2;
24) plot two graphs $I_{DS} = f(U_{DS})$, label each plot for the specific gate-source voltage ($U_{GS} = 0.5$ V and $U_{GS} = -1.5$ V) and name this graph Fig. 9.9;
25) verify, from the graph that the pinch-off saturation point voltage U_P was reduced by an increase in the bias voltage U_{GS}.

ELECTRICAL DIAGRAMS

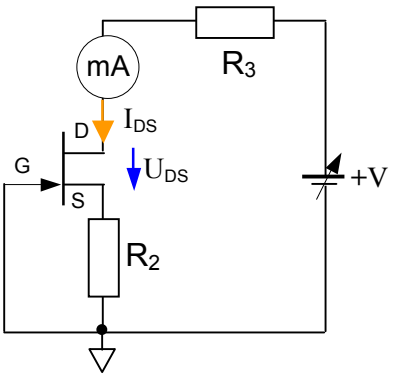

Fig. 9.7a

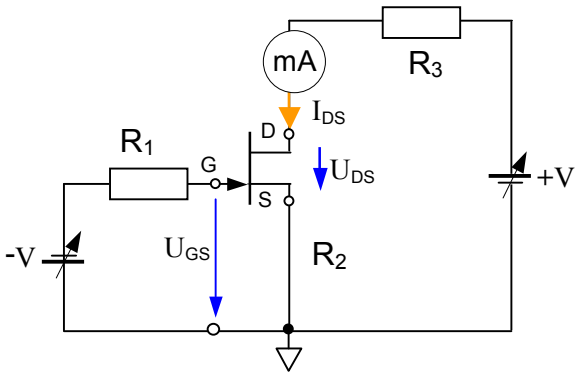

Fig. 9.7 b

6. Results:

See “procedure”
3 tables: Tab. 9.1a, Tab. 9.1b and Tab. 9.2
3 figures with graphs: Fig. 9.8a, Fig. 9.8b and Fig. 9.9

7. Discussions &Conclusions:

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Operational Amplifier as Comparator

1. Objective:

- Understand how operational amplifiers can be used as comparators
- Learn design techniques for operational amplifiers.

2. Equipment & Instruments

DC Supply Source
Function Generator
Oscilloscope
Multimeter
Breadboard
741 Opertional Amplifiers
Photodiode
LEDs
Resistors

3. Procedure

1. Build an operational amplifier circuit using only +!5V, -15V and GND as follows:
    a. Using a voltage divider create a +2V (approximately) and connect it to the inverting input of the op-amp.
    b. Using a 10k potentiometer and a resistor create a variable voltage (between 0V and 5V) and connect it to the non-inverting input of the operational amplifier.
    c. Set the output of the potentiometer to 0V. Measure the output of the op-amp.
    d. Increase the output of the potentiometer by 0.5V and measure the output of the op-amp again.
    e. Repeat step (d) until you have reached +5V.
    f. Draw conclusions.
2. Remove the +2V input in the previous circuit and insert a sinusoidal wave (4Vpp, 1kHz).
    a. Check the output of the op-amp on an oscilloscope. What do you see? Explain Why.
    b. Adjust the potentiometer up and down. What do you see on the oscilloscope? Explain Why.
3. Change the -15V supply source on the operational amplifier to GND. What changes?
4. Using a photodiode, green LED, yellow LED, Red LED, opamps and resistors. Design and build a 4-level light intensity detector. At Darkness no LEDS should come on, then as there is more light, the green LED should come on, followed by the yellow LED and finally the red LED.