German- Jordanian University

School of Electrical Engineering and Information Technology

Digital Electronics Laboratory

ECE 5420

Updated version of Dr. Mansour Abbadi manual

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German Jordanian University
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Laboratory Experiment (1)

Multiplexers and De-multiplexers

Objectives

To analyze the logic operation of a 4 lines to 1 line multiplexer (data selector) circuit and a 1 line to 4 line de-multiplexer circuit.

Instruments

DL 3155M18 module (unit #3), pulse generator, logic probes, logic switches, and a cable set.

Theory

The multiplexer (MUX), or data selector, is a digital device that is able to select one of several input signals according to a certain selection control and passes it to the output. Therefore, MUX has the ability to serialize the output data that are presented as parallel inputs. For a multiplexer, it is necessary to define the following inputs:

- ✓ **Data inputs:** the inputs where the data are sent in parallel**.**
- ✓ **Enabling input**: the input which inhibits or enables the transfer of the data from one of the inputs to the output.
- ✓ **Selection inputs:** the control inputs which are used to select the data inputs**.**

The relationship between the number of the selection inputs and the number of data inputs is represented by

$$Number\ of\ input\ data\ =\ 2^{Number\ of\ selection\ inputs}$$

For example, if the data inputs are eight, then three selection inputs are necessary since we have $2^3 = 8$ different binary combinations that can select all the eight data inputs. Let's now analyze the logic operation of a 4 lines to 1 line multiplexer. The symbol of the multiplexer is shown in Fig. 1.1 (IEC 617-12 rules) and the logic diagram is shown in Fig. 1.2, while the truth table is shown in Table 1.1.

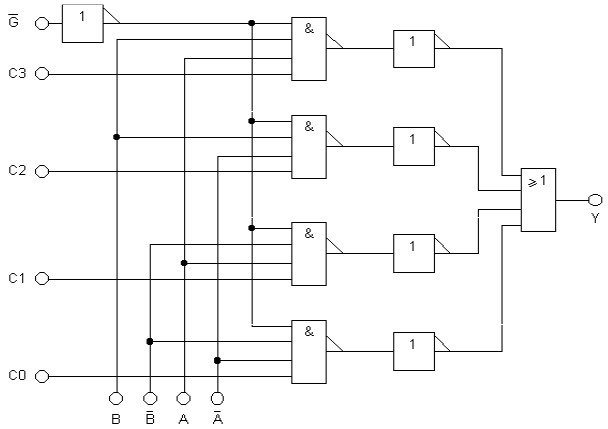

Fig. 1.1

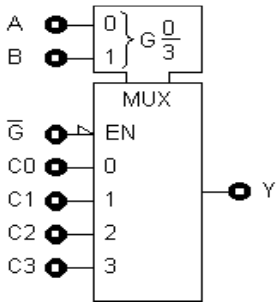

Fig. 1.2

INPUTS							OUTPUTS
ENABLE	SELECTION		DATA				
$\overline{G}$	B	A	C_3	C_2	C_1	C_0	Y
1	X	X	X	X	X	X	0
0	0	0	X	X	X	0	0
0	0	0	X	X	X	1	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	1	1	0	X	X	X	0
0	1	1	1	X	X	X	1

Table 1.1

From the simultaneous analysis of the truth table and the logic diagram, the following **conclusions** can be deduced.

- ✓ When logic "1" is applied to the enabling input, the circuit operation is completely blocked and the output is fixed at the logic value "0". This comes directly from the fact that all the NAND gates are disabled since enabling input is **active low**. In this case, it has no meaning to specify the logic signals present at all the other inputs and it is shown as indifference condition X.

- ✓ When logic "0" is applied to the enabling input, the circuit is enabled since the enabling input is **active low** so when there is the binary combination A = 0 and B = 0 on the selection inputs, the input C_0 is selected and therefore the logic value present on this input is transferred to the output; precisely: if $C_0 = 0$ then Y = 0 and if $C_0 = 1$ then Y = 1. In this case, it has no meaning to specify the logic signals on the other three not selected inputs, which are shown as indifference condition X. Quite similar arguments can be done to explain the operation of the multiplexer in case of the three remaining binary combinations of the selection inputs.

Demultiplexer

A demultiplexer (DMUX), or distribution frame, is seen as the opposite of the multiplexer. We can state that a demultiplexer is a circuit with one input and many outputs which is in contrary to the multiplexer. For a demultiplexer it is necessary to define the following inputs:

- ✓ **Data inputs**: the input where the data is applied.
- ✓ **Enabling input**: a control input that inhibits or enables the transfer of the input data to one of the outputs.
- ✓ **Selection inputs**: the control inputs dedicated to the selection of the desired output

The relationship between the number of selection inputs and the number of data outputs is represented by:

$$Number\ of\ output\ data\ =\ 2^{Number\ of\ selection\ inputs}$$

The symbol of a demultiplexer is shown in Fig. 1.3 (IEC 617-12 rules). Let's now analyze the logic operation of a 1 line to 4 lines demultiplexer whose logic diagram is shown in Fig. 1.4, while the truth table is shown in Table 1.2.

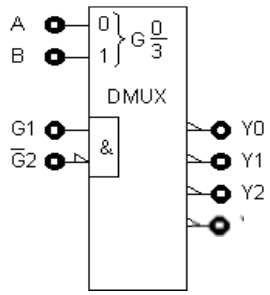

Fig. 1.3

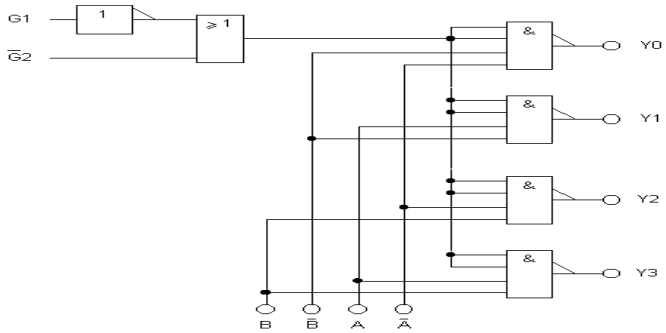

Fig. 1.4

INPUTS				OUTPUTS			
ENABLE	SELECTION		DATA				
$\overline{G2}$	B	A	G_1	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
1	X	X	X	1	1	1	1
X	X	X	0	1	1	1	1
0	0	0	1	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	1	1	0	1	1
0	1	1	1	0	1	1	1

Table 1.2

From the simultaneous analysis of the truth table and the logic diagram, one can deduce the following:

- ✓ The outputs are active low , so logic value "1" means OFF and logic value "0" means ON.
- ✓ All the outputs go to the logic value "1" in two different cases:
    - When the enabling input is set to the logic value "1" since the enabling input is **active low**.
    - When the input data is set to the logic value "0".

In both cases, the circuit operation is independent from the logic values present at all other inputs. The following analysis assumes that the enabling input is kept at logic level "0" and the input of the data G1 is kept at logic level "1". When A = 0 and B = 0, the output Y0 that assumes the logic value "0" is selected, while on the other remaining outputs the logic value "1" is present. Quite similar arguments can be developed to explain the operation of the demultiplexer for the three remaining binary combinations of the selection inputs.

PreLab

1. Simulate the circuits in Fig 1.5 and Fig. 1.6 and write the results in Table 1.3 and Table 1.4.
2. Prepare a short report with simulation results.

Procedure

Electrical Diagrams

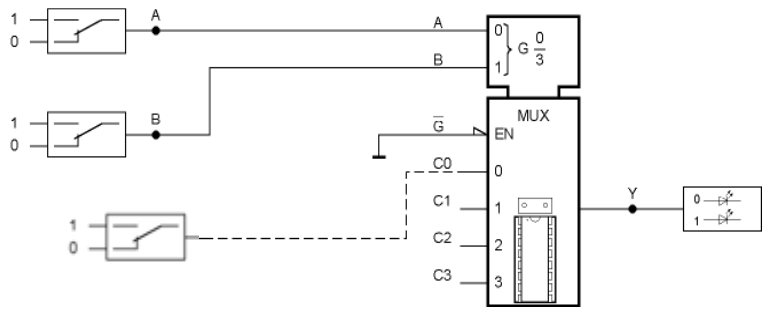

Fig. 1.5

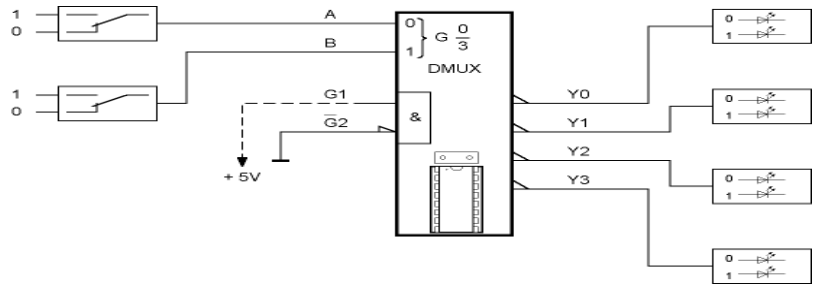

Fig. 1.6

Experiment

1. Insert Module 18 in the console and set the main switch to ON.
2. Connect the circuit shown in Fig. 1.5.
3. Connect the circuit inputs to switches and set the values according to Table 1.3. **NOTE**: It has no meaning to specify the logic signals which are shown as indifference condition X, so you may leave them without any input.
4. Verify that the output logic values are in conformity with the ones shown in the truth table (Table 1.1).
5. Remove all the connections.

INPUT							OUTPUT
ENABLE	SELECTION		DATA				
$\bar{G}$	B	A	C_3	C_2	C_1	C_0	Y
1	X	X	X	X	X	X	
0	0	0	X	X	X	0	
0	0	0	X	X	X	1	
0	0	1	X	X	0	X	
0	0	1	X	X	1	X	
0	1	0	X	0	X	X	
0	1	0	X	1	X	X	
0	1	1	0	X	X	X	
0	1	1	1	X	X	X	

Table 1.3

6. Connect the circuit shown in Fig 1.6 and connect its inputs to switches and set the values according to the Table 1.4.

7. Verify that the output logic values are in conformity with the ones shown in the truth table (Table 1.2)
8. Remove all the connections.

INPUT				OUTPUT			
ENABLE	SELECTION		DATA				
G_2	B	A	G_1	Y_3	Y_2	Y_1	Y_0
1	X	X	X				
X	X	X	0				
0	0	0	1				
0	0	1	1				
0	1	0	1				
0	1	1	1				

Table 1.4

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Laboratory Experiment (2)

R-S and J-K Flip-Flops

Objectives

To study the construction and verify the operation of the R-S and the J-K flip-flops

Instruments

DL 3155M20 module (unit #2), logic switches, logic probes, bounce-free switches, and cable set.

Theory

R-S Flip-Flop

The R-S F.F. is the simplest F.F. which consists of two inputs, called SET (shortened with S) and RESET (shortened with R), and two outputs, marked with Q and $\overline{Q}$ that assume normally opposite logic values. The input S is used to set the output Q to the logic level "1", while the input R is used to set the same output Q to the logic level "0". An R-S F.F. can be built using either two NOR gates or two NAND gates. These two different circuits are different only for the different logic values that have to be applied to the inputs to get the wanted output. In other words, NOR gates are used if the inputs are active high and NAND gates are used if the inputs are active low. The R-S F.F. circuit using two NAND gates is shown in Fig. 2.1. The truth table for the R-S F.F. by using NOR gates (active high) is shown in Table 2.1. The R-S F.F circuit using two NOR gates can built by simply replacing the NAND gates by NOR gates. The logic symbols for the two R-S F.F. are shown in Fig. 2.2 according to the rules of IEC 617-12. Finally, we can understand the logic operation of the R-S F.F. which uses NOR gates from the timing diagram of Fig. 2.3.

From the truth table, we can conclude that there are four states of the R-S F.F.:

- ✓ Hold: when R and S inputs are zeros in the **active high** or when R and S are ones in **active low**, the output of the flip flop is not changed and remains as the previous output.
- ✓ Set: when S is one and R is zero in **active high** or when S is zero and R is one in **active low**, the output of the flip flop is always one and the previous output does not affect the current output.

- ✓ Reset: when S is Zero and R is one in **active high** or when S is one and R is Zero in **active low**, the output of the flip flop is always zero and the previous output does not affect the current output.
- ✓ Undetermined : when R and S inputs are ones in the **active high** or when R and S are zeros in **active low**, the output of the flip flop is undefined. The undefined output is represented by "do not care" symbol X.

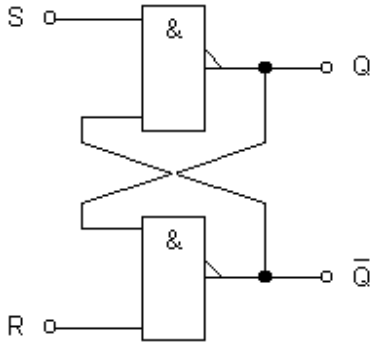

Fig. 2.1

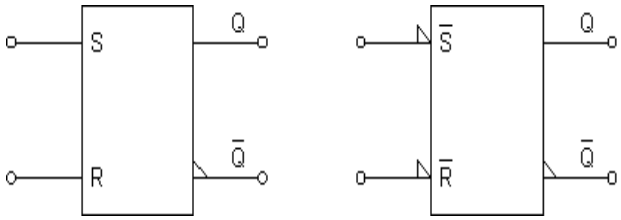

Fig. 2.2

INPUTS		PREVIOUS STATUS		OUTPUTS	
S	R	Q_0	$\overline{Q}_0$	Q	$\overline{Q}$
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	X	X
1	1	1	0	X	X

Table 2.1

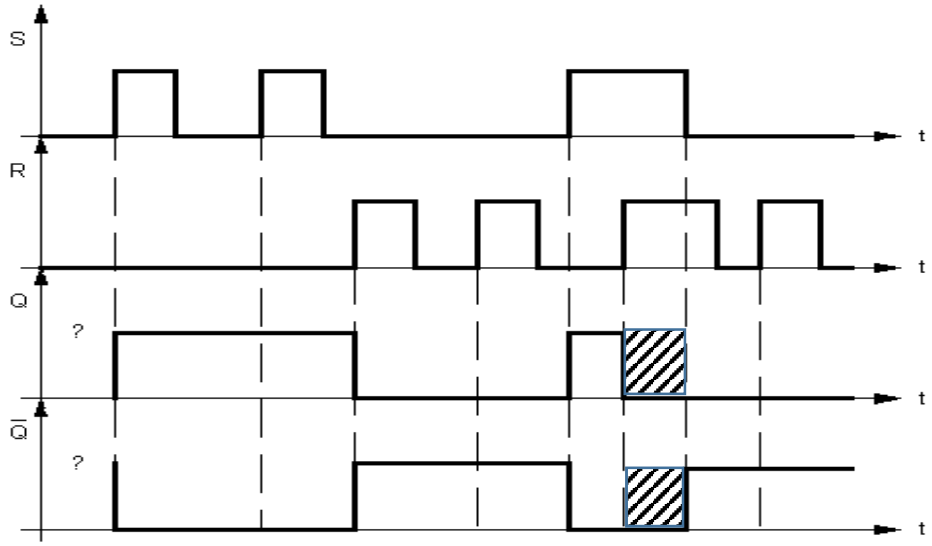

Fig. 2.3 R-S flip-flop timing diagram

J-K Flip-Flop

We have seen that an R-S F.F. has the disadvantage that its output state is undetermined when its two inputs signals have logic value "1" at the same time. This problem can be solved by adding two NAND gates to the input of the R-S F.F. as shown in Fig. 2.4 and the resulting F.F. is called J-K F.F. The truth table of J-K F.F is shown in Table. 2.2.

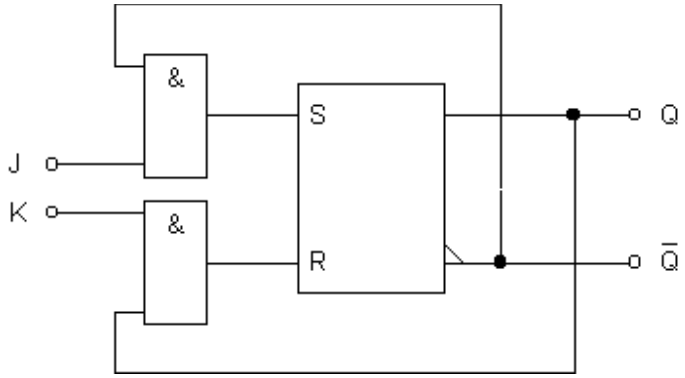

Fig. 2.4

INPUTS		PREVIOUS STATUS		OUTPUTS	
J	K	Q_0	$\overline{Q}_0$	Q	$\overline{Q}$
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

Table 2.2

From the truth table, we can conclude that there are four states of the J-K F.F

- ✓ Hold: when J and K inputs are zeros in the **active high** or when J and K are ones in **active low**, the output of the flip flop is not changed and remain as the previous one.
- ✓ Set: when J is one and K is zero in **active high** or when J is zero and K is one in **active low**, the output of the flip flop is always one and the previous output does not affect the current output.
- ✓ Reset: when J is zero and K is one in **active high** or when J is one and K is zero in **active low**, the output of the flip flop is always zero and the previous output does not affect on the current output.
- ✓ Toggle:when J and K inputs are ones in the **active high** or when J and K are zeros in **active low**, the output of the flip flop is opposite of the previous one.

J-K F.F. has a problem that it is unstable when the two inputs are both high and the duration of the input pulses are greater than the switching time of the gates. In this case, the output starts to oscillate between high and low. For this reason we prefer to release the control pulses from rigid duration limits, by introducing a third synchronization input called the TRIGGER or CLOCK and commonly marked with T or CLK as shown in Fig. 2.5. When the CLK is at logic level "1", the AND gates are enabled and the input signals can have the F.F. switched. On the contrary, when the CLK is at logic level "0", the AND gates are blocked and the F.F. is disconnected from the closed loop of output-input cyclic reaction.

The outputs of a J-K F.F. can switch either in response to a rising edge and it is called **positive-edge triggered flip-flop** or to a falling edge and it is called **negative edge-triggered flip-flop**. The logic symbols for both types of clocked J-K F.F. are shown in Fig. 2.6 and Fig. 2.7; respectively, according to the Rules of IEC 617-12.

The logic operation of the two different J-K flip-flop can be described by the two truth tables shown in Table 2.3 and Table 2.4. The logic operation of the two types of J-K F.F. can be easily understood from the timing diagrams shown Fig. 2.8 and Fig. 2.9, respectively**.**

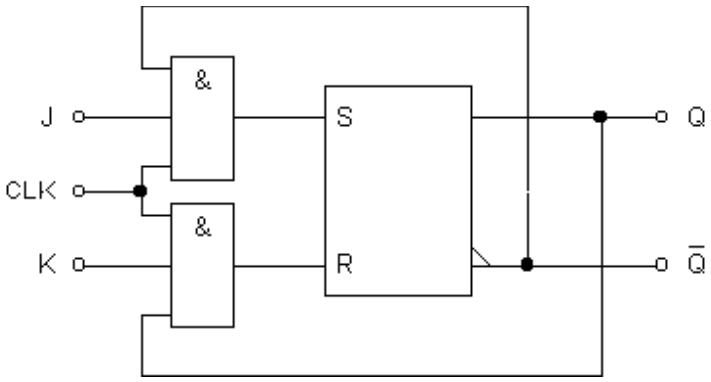

Fig. 2.5

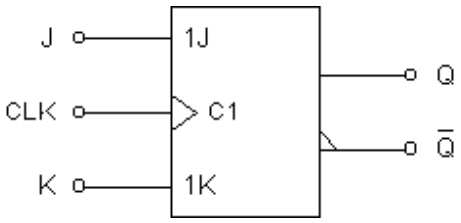

Fig. 2.6

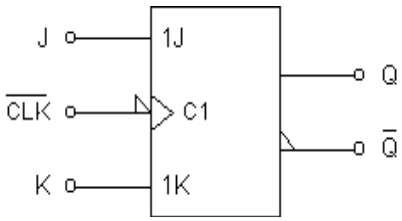

Fig. 2.7

INPUTS			**OUTPUTS**		
CLK	**J**	**K**	Q	$\overline{Q}$	
↑	**0**	**0**	Q_0	$\overline{Q}_0$	**The upwards arrow represents the switching on the rising edge**
↑	**0**	**1**	**0**	**1**	
↑	**1**	**0**	**1**	**0**	
↑	**1**	**1**	$\overline{Q}_0$	Q_0	

Table 2.3

INPUTS			**OUTPUTS**		
CLK	**J**	**K**	**Q**	$\overline{Q}$	
↓	**0**	**0**	Q_0	$\overline{Q}_0$	**The downwards arrow represents the switching on the falling edge**
↓	**0**	**1**	**0**	**1**	
↓	**1**	**0**	**1**	**0**	
↓	**1**	**1**	$\overline{Q}_0$	Q_0	

Table 2.4

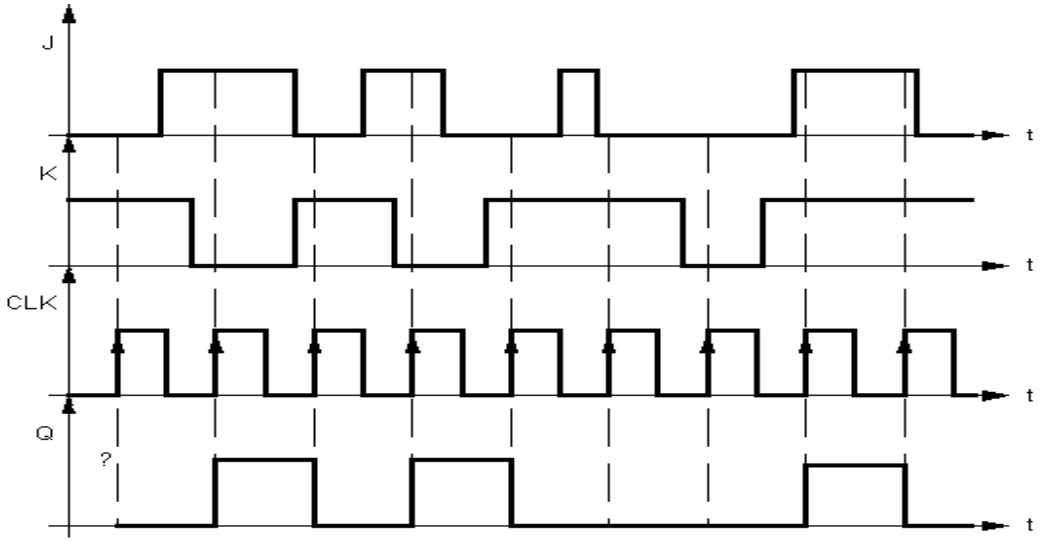

Fig. 2.8

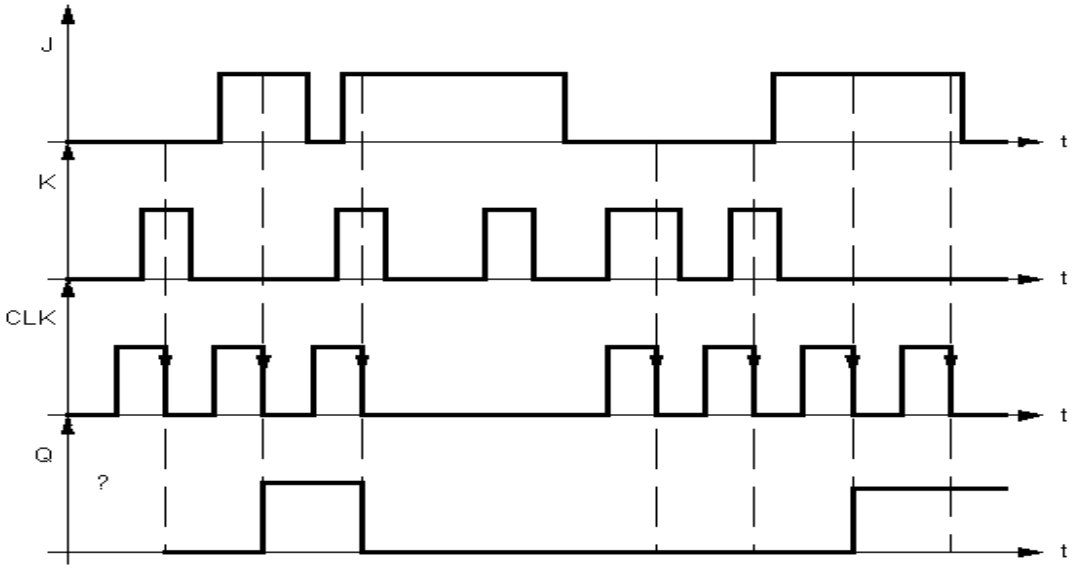

Fig. 2.9

The J-K F.F. is normally provided with two further inputs, called PRESET or SET and CLEAR or RESET - shortened PRE or S and CLR or R, that are necessary to set the outputs respectively to the logic level “1” or to the logic level "0".

While the J and K inputs allow a SYNCHRONOUS OPERATION of the F.F. because it is synchronized with the CLK signal, the PRE and CLR inputs allow an ASYNCHRONOUS OPERATION because there are independent of the sequence of the CLK signals. For this reason, the J, K and CLK inputs are called SYNCHRONOUS INPUTS while the PRE and CLR inputs are logic level “0” called ASYNCHRONOUS INPUTS. For all J-K F.F. the asynchronous inputs have a greater priority as to the synchronous inputs.

The logic operation of the F.F. outputs as a function of the PRE and CLR inputs can be explained by the truth table shown in Table 2.5. Generally we prefer to define the logic operation of a J-K F.F. with a single truth table, like the one shown in Table 2.6.

ASYNCHRONOUS INPUTS		SYNCHRONOUS INPUTS			OUTPUTS	
PRE	**CLR**	**CLK**	**J**	**K**	Q	$\overline{Q}$
0	**0**	x	x	x	Depend on J-K and CLK	
0	**1**	x	x	x	**0**	**1**
1	**0**	x	x	x	**1**	**0**

Table 2.5

INPUTS					OUTPUTS	
PRE	**CLR**	**CLK**	**J**	**K**	Q	$\overline{Q}$
1	0	X	X	X	**1**	**0**
0	1	X	X	X	**0**	**1**
1	1	X	X	X	**X**	**X**
0	0	↑	0	0	Q_0	$\overline{Q}_0$
0	0	↑	1	0	**1**	**0**
0	0	↑	0	1	**0**	**1**
0	0	↑	1	1	**TOGGLE**	
0	1	0	X	X	Q_0	$\overline{Q}_0$

Table 2.6

Prelab

1. Simulate the circuit in Fig 2.10 and Fig. 2.11. Write the results in Table 2.7 and Table 2.8.
2. Prepare a short report with simulation results.

Procedure

1. Insert Module 20 in the console and set the main switch to ON.
2. Connect the circuit shown in Fig. 2.10:
   - ✓ Connect the outputs A and B of the BOUNCE-FREE SWITCHES to the inputs R and S of the R-S flip-flop.
   - ✓ Connect the outputs Q and $\bar{Q}$ of the flip-flop to the inputs IN_1 and IN_2 of the LOGIC PROBES (LP).
3. Set the switches A and B of the BOUNCE-FREE SWITCHES to generate respectively all the logic signals for the inputs S and R of the flip-flop and write the output in Table 2.7.
4. Draw in Fig. 2.11 the timing diagram of the output.
5. Remove all the connections.

Electric Diagrams

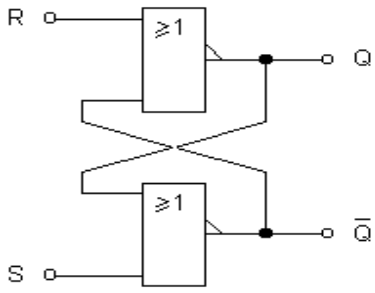

Fig.2.10

Results

INPUTS		PRESENT STATE	OUTPUTS	
S	**R**	**Q_0**	**Q**	**Q'**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

Table 2.7

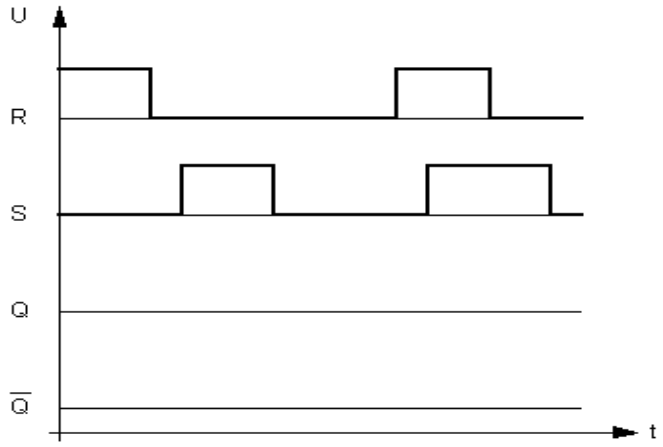

Fig. 2.11

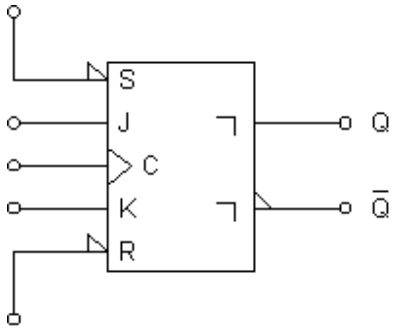

Fig.2.12

Experimentation

1. Insert Module 20 in the console and set the main switch to ON.
2. Connect the circuit as shown in Fig. 2.12:
   - ✓ Connect output A of the BOUNCE-FREE SWITCHES to input C of the J-K flip-flop.
   - ✓ Connect the outputs A, B, C and D of the LOGIC SWITCHES (LS) respectively to S, R, J and K of the J-K flip-flop.
   - ✓ Connect the outputs Q and Q of the flip-flop to the inputs IN1 and IN2 of the LOGIC PROBES (LP).

3. Set the switches to reproduce all the input logic states of the J-K flip-flop, and write the output logic signals in Table 2.8.
4. Draw in Fig.2.13 the timing diagram of the output.
5. Remove all the connections.

Obtained results

INPUTS					OUTPUTS	
CLR (R)	**PRE (S)**	**C**	**J**	**K**	Q	$\overline{Q}$
0	**1**	**X**	**X**	**X**		
1	**0**	**X**	**X**	**X**		
0	**0**	**X**	**X**	**X**		
1	**1**	⎍	**0**	**0**		
1	**1**	⎍	**0**	**1**		
1	**1**	⎍	**1**	**0**		
1	**1**	⎍	**1**	**1**		

Table 2.8

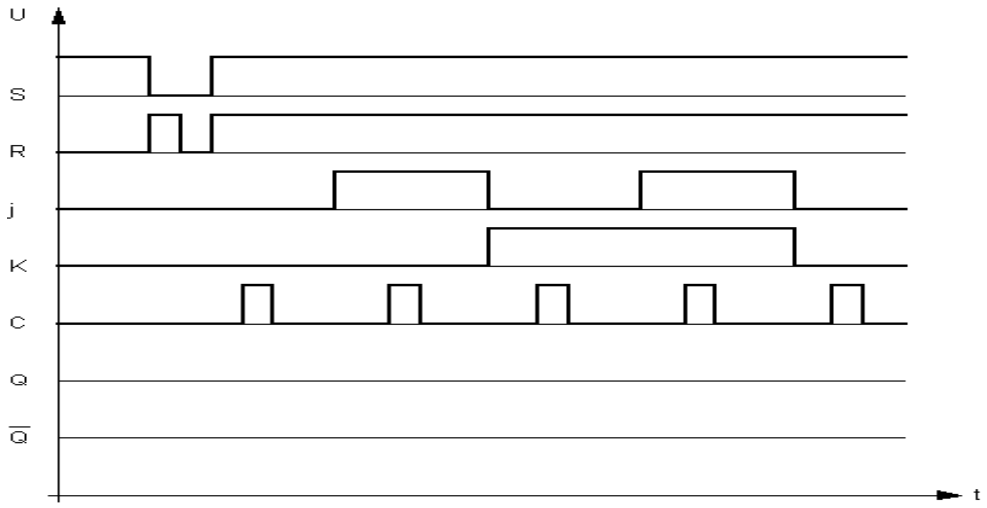

Fig. 2.13

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Laboratory Experiment (3)

Electric Characteristics of the TTL Logic gates

Objectives
To determine by direct measurements the low and high levels of the input/output voltages and currents for the TTL logic gates.

Instruments
DL 3155M18 module (unit # 4), Oscilloscope, Signal generator, two digital multi-meters, and cable set.

Theory
The most widely used logic family in digital electronics is the TTL (Transistor-Transistor Logic) one. TTL is a technology that uses integrated bipolar transistors to build both combinational and sequential logic functions. It is composed of two series, commercial and military, that are designed to work under different operating temperature ranges. In each series, there are also different subfamilies with different characteristics, such as different power absorptions, different switching times, etc. The basic component in this family is the **BJT** transistor, which is used as a switch that operates in the cutoff and the saturation states only. Fig.3.1 shows the circuit diagram of a TTL inverter; the transistor V1 and the diode V6 are, respectively, the coupling transistor and the input clamping diode. The transistor V2 is called the phase splitter, while the combination of the two transistors V3 and V4 composes the output circuit.

This circuit is defined as totem-pole structure. The diode V5 assures that transistor V3 is in cutoff when V4 is in saturation, i.e., when there is a high logic state at the gate input. In this case, the collector voltage of V2 is equal to the voltage VBE of V4 plus the voltage VCE of V2 which is equal to 1 V. The diode V5 provides a further voltage drop, equal to VBE, in series with the base-emitter junction of V3, to assure that such a transistor goes in cutoff when V4 is in saturation. The function, on the contrary, of the diode V6 is to avoid negative voltage spikes present at the input of the gate which may damage V1.

Each logic family has its own characteristic parameters, which must be specified before using its gates in any application. One of the most important parameters is the **supply voltage** over which the gate can work without problems. In TTL family, it is 5 V with a tolerance of 5 % while in CMOS it can be 5 or 15 V. The second parameter is the **voltage and current levels** of the low logic and high logic inside which a right operation is

guaranteed. The third parameter is the **power dissipation** of the gate, which is the product of the supply voltage by the current it supplies to the gate when it is in the low and high states then taking the average. The fourth parameter is the **propagation delay**, which is the time interval between the instant of applying the input pulse to the gate and the instant of getting the pulse at the output of the gate. The fifth parameter is **noise margin**, which is an indicator of the ability of the gate to work under noisy conditions without error. The sixth parameter is the **fan-out**, which is the number of gates, which can be driven by the gate without affecting its performance.

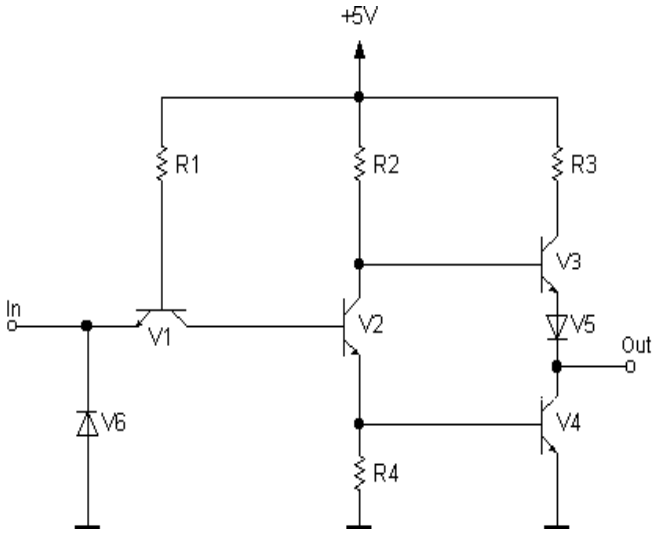


Fig. 3.1

Noise Margins

Digital logic gates operate in two logic states only, which are the low logic (logic-0) and high logic (logic-1). It is necessary when cascading these gates that the low level at the output of the driving gate is understood as a low level by the driven gate and the same thing is valid for the high level. The range of voltages, which appear at the input and the output of the gates under different operating conditions identify the low and high levels and they are determined from the input-output transfer characteristics of the gates. From Fig. 3.2, for logic-1 to be understood by cascaded gates, the worst case high output voltage of the driving gate (V_{OH}) must be greater than the worst case input high voltage (V_{IH}) of the driven gate. For logic-0 to be understood by cascaded gates, the worst case low output voltage of the driving gate (V_{OL}) must be less than the worst case low input voltage (V_{IL}) of the driven gate. **The ability of digital logic gates to maintain their operation without error under varying voltage levels and in the presence of noise from different sources is measured by noise margins (NM).** The low and high noise margins are defined as:

$NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$

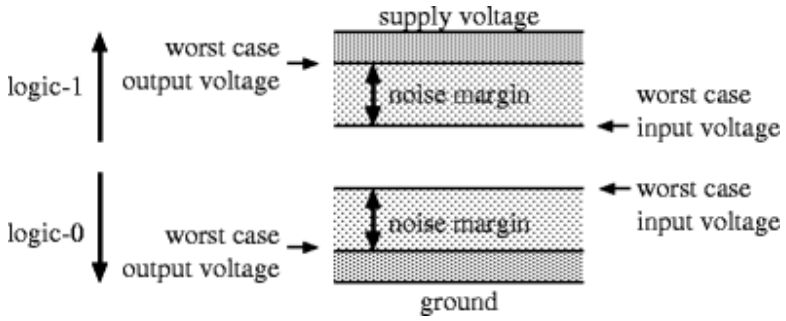


Fig. 3.2

Prelab

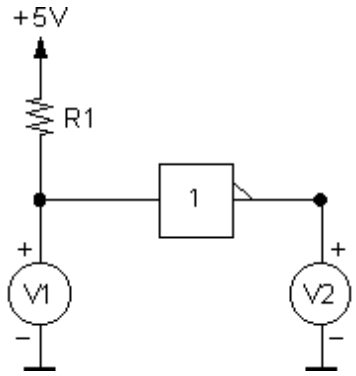
- ✓ Simulate all the circuits from Fig 3.3 to Fig 3.10.
- ✓ Prepare a short report with simulation results.

Procedure

Components: R1, R2, R3, R4 = 1 KΩ – 1/4 W- 5%, R5= 100 KΩ potentiometer.

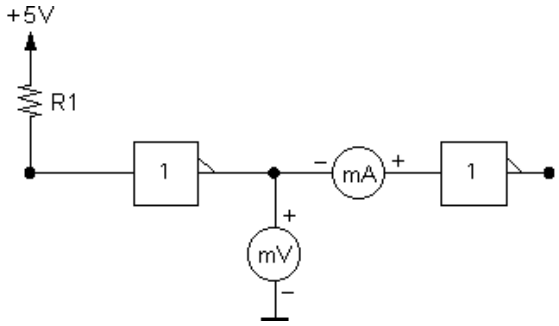
EXPERIMENT

- ✓ Insert Module 18 in the console and set the main switch to ON.
- ✓ Connect the following circuits, read the indications of the multi-meters and write them in the corresponding table.



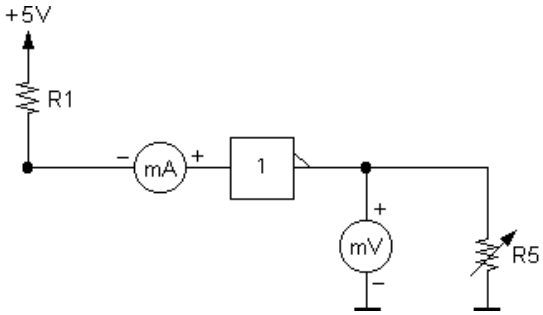
Vin [V]	Vout [V]

Fig. 3.3



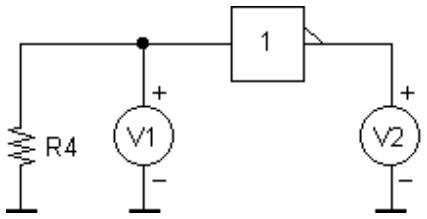
Vout [V]	Iin [µA]

Fig. 3.4



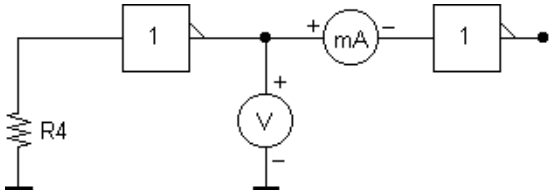
R5	Iin [µA]	Vout [V]
5K		
50K		
100k		

Fig. 3.5



Vin [V]	Vout [V]

Fig. 3.6



Vout [V]	Iin [µA]

Fig. 3.7

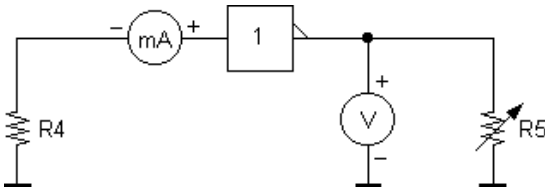


Fig. 3.8

R5	Iin [µA]	Vout [V]
5K		
50K		
100k		

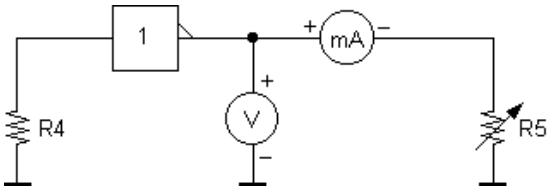


Fig. 3.9

R5	Iout [µA]	Vout [V]
5K		
50K		
100k		

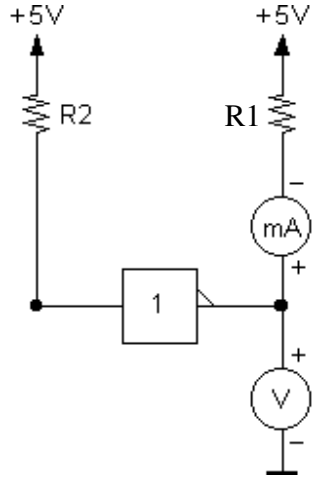


Fig 3.10

Vout [V]	Iout [µA]

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Laboratory Experiment (4)

TTL Logic Family

Objectives

To understand how an inverter circuit works and determine the voltage transfer characteristics, and the average propagation time of TTL logic family.

Instruments

DL 3155M18 module (unit #5), logic switches, oscilloscope, signal generator, digital multi-meters, and cable set.

Theory

The construction of the TTL inverter was discussed in Experiment (3). Let's now examine the operation of the TTL inverter, when its input is either in high or low logic levels.

As we can observe from Fig. 4.1, when a high logic level is present, the base-emitter junction of V1 is inversely biased, while the base-collector one is directly biased. In this situation, the current after having crossed the resistance R1 and the base-collector of V1, arrives to the base of V2 carrying it to saturation. Moreover, V4, owing to the state of V2, goes onto saturation while V3 onto cut off state and V5 go to reverse bias since the collector voltage of V2 has a low voltage. Therefore, the output voltage is in low state since it is connected to ground since V4 is in saturation and disconnected from V_{CC} since V3 and V5 are OFF. When, on the contrary, there is a low logic level at the input, the base-emitter junction of V1 is directly biased, while the base-collector is inversely biased. In this case, the current crossing R1 and the base-emitter junction of V1 goes towards the ground. The transistor V2, whose base has a zero current, goes to cutoff state and consequently V4 goes to cutoff state. Since V2 is OFF, the base of V3 is connected to V_{CC} through R_2 and therefore it will be on and moreover the diode V5 is on. Since the output is isolated from ground because V4 is OFF and connected to V_{CC} because V3 and V5 are ON, it will be in the high state. We conclude that when the input has a high logic level, the output is at a low logic level and vice versa, and therefore this gate works as an inverter.

The diode V5 assures that transistor V3 is in cutoff, when V4 is in saturation, i.e. when there is a high logic state at the gate input. In this case, the collector voltage of V2 is equal to the voltage VBE of V4 plus the voltage VCE of V2 which is equal to 1 V. The diode V5 provides a further voltage drop, equal to VBE, in series with the base-emitter junction of V3, to assure that such a transistor goes in cutoff when V4 is in saturation. The function, on the contrary, of the diode V6 is to avoid negative voltage spikes present at the input of the gate which may damage V1.

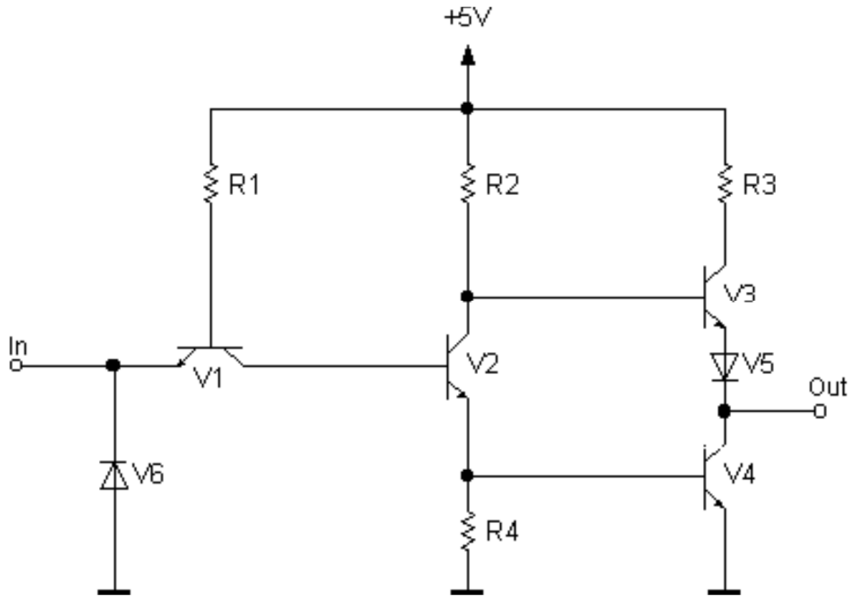

Fig. 4.1

Transfer Characteristics

The different parameters of a logic gate such as noise margins can be determined from its transfer characteristics which is a plot of the output voltage as function of the input voltage over the range from zero to the supply voltage. The transfer function is divided into three regions which are the high level region, the low level region and the transition region as shown in Fig. 4.2. The smaller the transition region, the better will be the characteristics since it gives higher noise margin especially when the transition region is located halfway between the supply voltage and the ground. The width of the transition region V_{TW} and the logic swing V_{LS} are defined as:

V_{TW}= V_{IH} - $V_{IL,}$ and V_{LS} = V_{OH} – V_{OL}.

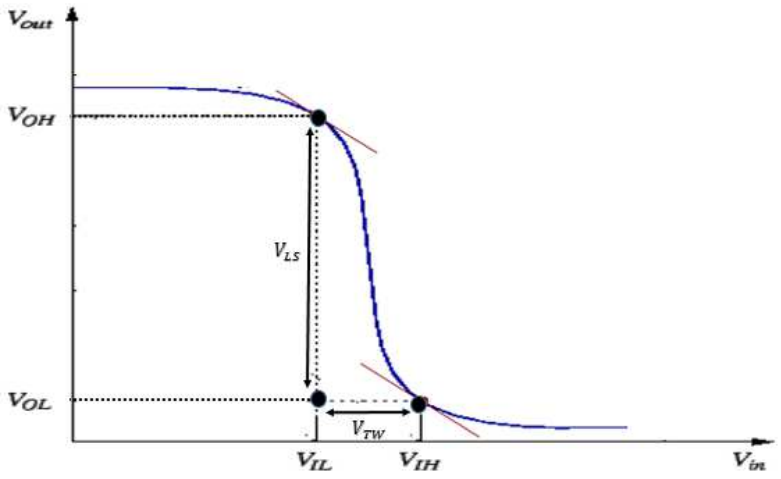

Fig. 4.2

Prelab

1. Simulate the circuit in Fig 4.3 with the values mentioned below in the component list and write the results in Table 4.1.
2. Prepare a short report with simulation results.

Procedure

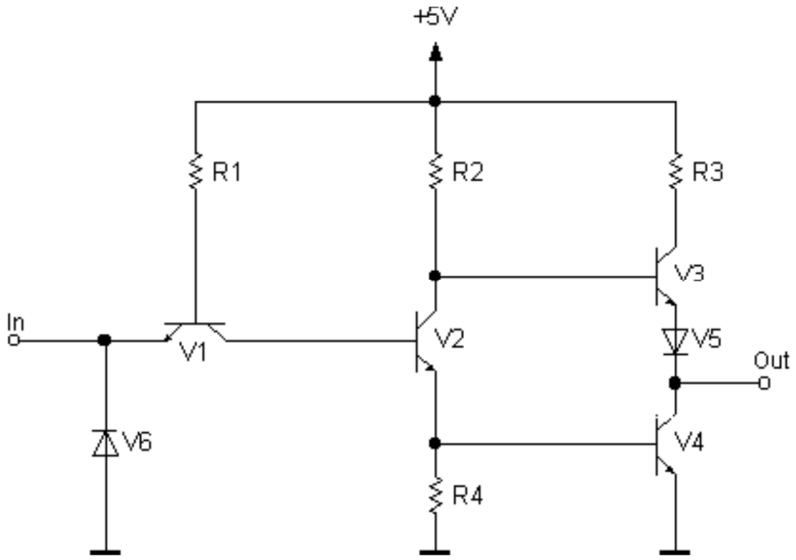

Fig. 4.3

Components List

R1 = 3.9 kΩ, R2 = 1.6 kΩ, R3 = 130 Ω, R4 = 1 kΩ. V1, V2, V3, V4 = 2N5550.
V5 and V6= 1N4148.

EXPERIMENT

1. Insert Module 18 in the console and set the main switch to ON.
2. Connect the circuit shown in Fig. 4.3.
3. Set the switch S1 to ON.
4. Connect the input of the logic gate (jack 1) to the output of the logic switch A.
5. Use voltmeter to determine the state of each transistor and diode by measuring the values shown in Table. 4.1 when the input is at logic state 0 and logic state 1.
6. Write the values read on the voltmeter in Table. 4.1.
7. Connect the output of the logic gate (jack 7) to the resistance R4 of block 4.
8. Repeat the operations of points 4 - 6 and write the values in Table. 4.1.

Vi	Vo	Vo with load R4	V2		V3		V4		V5	V6
			V_{BE}	V_{BC}	V_{BE}	V_{BC}	V_{BE}	V_{BC}		
0										
5										

Table. 4.1

TRANSFER CHARACTERISTICS OF A TTL GATE

1. Turn the potentiometer R6 completely counter clockwise to obtain an input voltage equal to 0 V.
2. Connect the circuit, and the multi-meters as shown in Fig. 4.4.
3. Adjust the potentiometer R6 for all the input voltage values shown in Table 4.2 and write the corresponding output voltage values.
4. Use the data in Table 4.2 to draw the transfer characteristics (V2 versus V1) of the TTL gate.

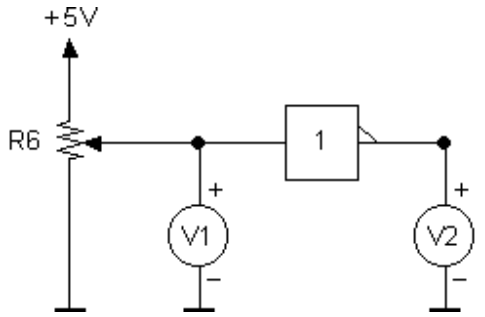

Fig. 4.4

V1	0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	2.8	3.0
V2																

Table. 4.2

PROPAGATION DELAY TIME OF A TTL GATE

1. Connect the circuit, the signal generator and the oscilloscope as in Fig. 4.5.
2. Adjust the oscilloscope in the following way: CH1 = 0.2 VOLT/DIV, CH2 = 0.2 VOLT/DIV, TIME/DIV = 0.2 ms, coupling = DC.
3. Adjust the function generator to generate a square wave signal with frequency = 1 MHz and Vpp = 5 V.
4. Determine the propagation delay of the TTL gates by using the cursors in the oscilloscope.

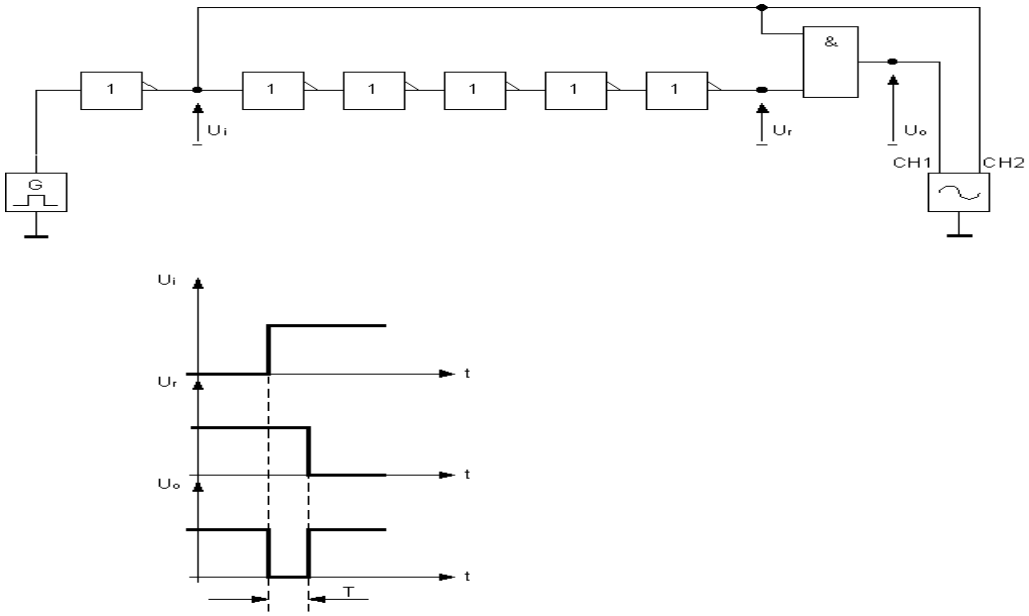

Fig. 4.5

Calculation data

Propagation time: $t_p = T/n$

where: n = number of the logic gates (5), and T = delay time of the 5 inverter chain

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Laboratory Experiment (5)

CMOS Logic Family

Objectives:

To determine the low and high levels of the input/output voltages, the voltage transfer characteristics, and the truth table for different CMOS logic gates.

Instruments:

DL 3155M18 module (unit #6), Oscilloscope, logic switches, two digital multi-meters, and cable set.

Theory:

The MOS (Metal Oxide Semiconductors) logic family can be used to build logic gates with **lower number of transistors** compared with the TTL logic family. Moreover the MOS transistor **occupies less area** on the chip which allows the highest integration density possible. The CMOS (complementary MOS) family is the most popular among the MOS family since it has the least power consumption which reaches to almost zero at rest (no switching). The basic structure of a CMOS gate is the inverter which is formed by connecting in series two complementary MOS transistors [PMOS (V1) and NMOS (V2)], that have similar electric characteristics as shown in Fig. 5.1. The source of the PMOS transistor is connected to the $+V_{DD}$ power supply (+5V), while the source of the NMOS transistor is connected to ground. When the inverter input is ground connected, i.e. at logic state "0", the PMOS transistor is in conduction state and the NMOS transistor is in cutoff state and therefore the output is high. On the contrary, when the input is connected to V_{DD} i.e. at logic level "1", the NMOS transistor is in conduction state while the PMOS transistor is in cutoff state and therefore the output is low. In both cases, one transistor only conducts and the other one is in cutoff, and therefore, the power consumption at rest, is extremely low.

CMOS inverters can be used to build other gates such as NAND and NOR gates. Fig. 5.2 shows the connection of a two input CMOS NAND gate where the NMOS transistors are connected in series while the PMOS transistors are connected in parallel. Fig. 5.3 shows the connection of a two input CMOS NOR gate where the NMOS transistors are connected in parallel while the PMOS transistors are connected in series which is the opposite connection of the NAND gate.

Procedure

Electrical Diagrams

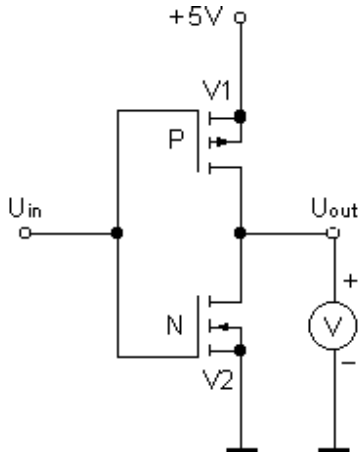

Fig. 5.1

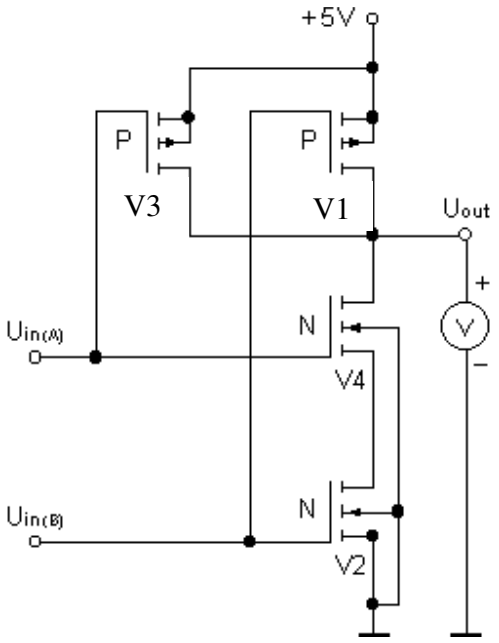

Fig. 5.2

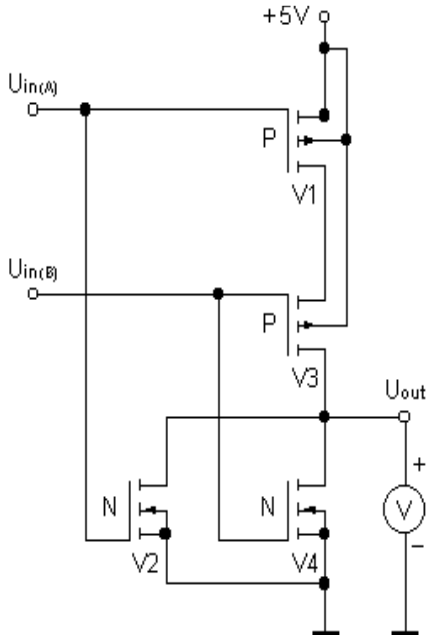

Fig. 5.3

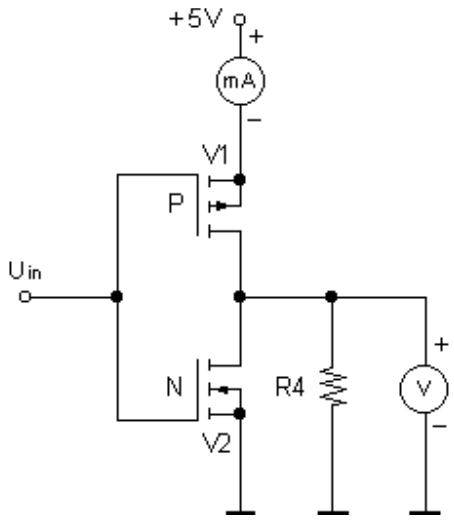

Fig. 5.4

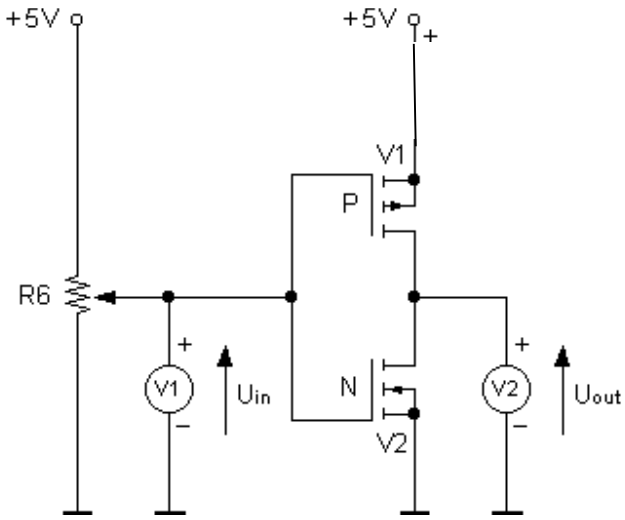

Fig. 5.5

Prelab

- ✓ Simulate all circuits from Fig. 5.1 to Fig. 5.5.
- ✓ Prepare a short report with simulation results.

Experiment

CMOS INVERTER

1. For the circuit shown in Fig. 5.1, set the switch S1 to close.
2. Connect the input of the logic gate (jack 6) to the output of the logic switch A.
3. Connect a voltmeter to the output of the logic gate.
4. Determine the voltage that is present at the output of the logic gate, when the input logic state is 0 and 1, respectively.
5. Write the values in Table. 5.1 and determine the type of the logic gate.
6. Set the switch S1 to Open.

CMOS NAND GATE

1. For the circuit in Fig. 5.2, set the switch S1 to close.
2. Connect the inputs of the logic gate (jacks 6 and 3) to the outputs of the logic switches A and B.
3. Determine the voltage that is present at the output of the logic gate, when the logic states written in Table. 5.2 are present at its inputs.
4. Write the values in Table. 5.2 and determine the type of the logic gate.
5. Set the switch S1 to Open and remove all the connections.

CMOS NOR GATE

1. For the circuit in Fig 5.3; set the switch S1 to ON;
2. Connect the inputs of the logic gate (jacks 6 and 3) to the outputs of the logic switches A and B.
3. Connect a multi-meter by setting the voltmeter to the output of the logic gate.
4. Determine the voltage that is present at the output of the logic gate, when at its inputs the logic states written in Table. 5.3 are present at its inputs.
5. Write the values in Table. 5.3 and determine the type of the logic gate.
6. Set the switch S1 to Open and remove all the connections;

CMOS POWER CONSUMPTION

1. Connect the circuit with the ammeter and the voltmeter as in Fig. 5.4, by keeping the switch S1 to OFF.
2. Connect the resistance R4 of block 4 to the inverter output.
3. Read the multi-meters indications, when both the logic zero and the logic 1 are present at its input, and write them in Table. 5.4.
4. Calculate the power absorbed by the inverter and write the result in Table. 5.4.
5. Remove all the connections and comment on the results.

CMOS TRANSFER CHARACTERISTICS

1. Connect the circuit with the two voltmeters as in Fig. 5.5 by keeping the switch S1 to OFF.
2. Turn completely clockwise the potentiometer R6 of block 4 to obtain an input voltage of 0 V.
3. Read the indications of the voltmeters (V_{IN}, V_{OUT}) and write them in Table. 5.5.
4. Adjust the potentiometer R6 for all the input voltage values written in Table.5.5 and read the output voltage values then write them in the same table.
5. Draw graphically the transfer characteristic of the CMOS gate, that describes the relation between the input and output voltages by calculating N_{mH} ,N_{mL}, V_{LS} and V_{TW}.
6. Remove all the connections and comment on the results.

V_{IN} [V]	V_{OUT} [V]
0	
+5	

Table 5.1

$V_{IN(A)}$ [V]	$V_{IN(B)}$ [V]	V_{OUT} [V]
0	0	
0	+5	
+5	0	
+5	+5	

Table 5.2

VIN(A) [V]	VIN(B) [V]	VOUT [V]
0	0	
0	+5	
+5	0	
+5	+5	

Table 5.3

VIN [V]	I [mA]	VOUT [V]	P [mW]
0			
+5			

Table 5.4

V_{IN} [V]	0.4	0.8	1.2	1.3	1.4	1.5	1.6	2.0	2.4	2.8	3.2	3.6	4.0	4.5
V_{OUT} [V]														

Table 5.5

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Laboratory Experiment (6)

Interfacing TTL and CMOS Logic Gates

Objectives

To verify the interfacing conditions between CMOS and TTL logic families and to be able to interface CMOS gate to TTL gate and vice versa.

Instruments

DL 3155M20 module (unit #4), 3 digital multi-meters, and cable set.

Theory

Interfacing means connecting together different digital circuits such as logic gates with different electrical characteristics. Sometimes, a direct connection between gates from different technologies is not possible and it is necessary to use an interfacing circuit between the driver gate and the driven gate. The following conditions must be satisfied in order to interface two gates from different logic families:

1. V_{OL} (driver) < V_{IL} (driven)
2. V_{OH} (driver) > V_{IH} (driven)
3. I_{OL} (driver) > -N I_{IL} (driven)
4. -I_{OH} (driver) > N I_{IH} (driven)

where N is the maximum number of the driven gates (fan-out).

If one or more of the above conditions are not satisfied, an interfacing circuit is needed between the driver and the driven gates. Table 6.1 shows the worst case voltages and currents for some TTL and CMOS families**.**

parameter	74H CMOS	74 TTL	74LS TTL	74AS TTL	74ALS TTL
V_{IH}	3.5 V	2 V	2 V	2 V	2 V
V_{IL}	1 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{OH}	4.9 V	2.4 V	2.7 V	2.7 V	2.7 V
V_{OL}	0.1 V	0.4 V	0.4 V	0.4 V	0.4 V
I_{IH}	1 µA	40 µA	20 µA	200 µA	20 µA
I_{IL}	-1 µA	-1.6 mA	-400 µA	-2 mA	-100 µA
I_{OH}	-4 mA	-400 µA	-400 µA	-2 mA	-400 µA
I_{OL}	4 mA	16 mA	8 mA	20 mA	4 mA

Table 6.1

Interfacing from CMOS to TTL

Let's now examine the case where a CMOS gate drives TTL gates. From the previous experiments, we saw that the value of the output voltage at HIGH level of the CMOS is V_{OH} = 4.9 V. Since this value is higher than the value of the input voltage at the HIGH level of the TTL (V_{IH} = 2 V), it follows that the CMOS is compatible with the TTL at HIGH level. In a similar way, always, the output voltage at LOW level of the CMOS assumes the value V_{OL} = 0.1 V. Since this value is lower than the value of the input voltage at LOW level of the TTL (V_{IL} = 0.8 V), it follows that the CMOS is compatible with the TTL in the LOW state too. In terms of currents, the CMOS at LOW output state can absorb 4 mA (I_{OL}). In case where it is driving some 74 standard TTL, the CMOS gate has to absorb from each TTL input 1.6 mA (I_{IL}). This fact limits the fan-out of the CMOS gate to two TTL gates only (4 mA/1.6 mA = 2.5). On the contrary, in the case we are driving some 74LS TTLS, the CMOS gate has to absorb from each TTL input, 0.4 mA (I_{IL}); this limits the fan-out of the CMOS gate to ten TTL gates (4 mA/0.4 mA = 10) as shown in Fig. 6.1. In case we are driving some 74AS TTL, the CMOS gate has to absorb from each TTL input, 2 mA (I_{IL}); this limits the fan-out of the CMOS gate with two TTL inputs (4 mA/2 mA = 2). Finally, in case we are driving some 74ALS TTL, the CMOS gate has to absorb from each TTL input, 0.1 mA (I_{IL}); this limits the fan-out of the CMOS gate at forty TTL inputs (4 mA/0.1 mA = 40).

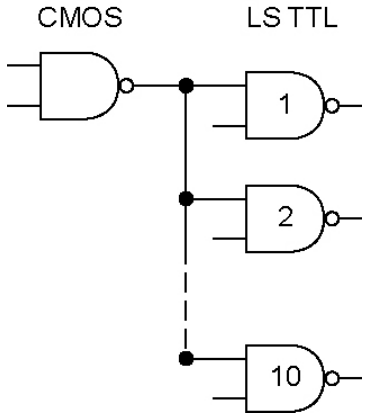


Fig. 6.1

Interfacing from TTL to CMOS

When a TTL gate has to drive CMOS gates, the interface is not as simple as in the above case. From the previous experiments, we saw that, in the LOW state the output voltages of the TTL and the input one of the CMOS are compatible for the interfacing. In the HIGH state, on the contrary, the TTL families are characterized by an output voltage value V_{OH} that goes from 2.4 V to 2.7 V, not enough to drive a CMOS that at HIGH state needs a voltage of V_{OH} = 3.5 V. Therefore, an interface is needed for a TTL gate to drive CMOS gates. The interface is a simple pull-up (Rp) resistance connected to a Vcc as shown in Fig. 6.2.

When the output voltage of the TTL gate is high, it will be pulled to 5V by the resistor. In the LOW state, the driver TTL gate has to absorb current both from the Rp resistance and from the CMOS inputs to which it is connected as shown in Fig. 6.3.

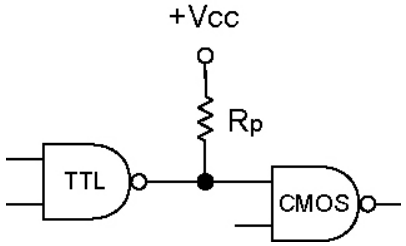


Fig. 6.2

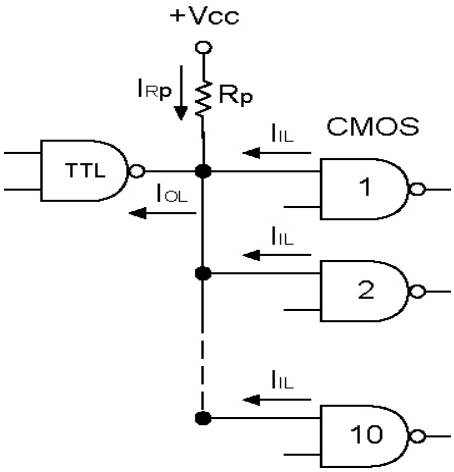


Fig. 6.3

From Fig. 6.3, we see that it is possible to obtain the minimum value of the resistance Rp which is necessary to interface these devices in the right way from the following relationships:

$$\boldsymbol{Rp} = (\boldsymbol{VCC} - \boldsymbol{V_{OL}}) / \boldsymbol{I_{Rp}}$$

$$\boldsymbol{I_{Rp}} = \boldsymbol{I_{OL}(TTL)} - \boldsymbol{n}\, \boldsymbol{I_{IL}(CMOS)}$$

where n is the number of CMOS gates and I_{Rp} is the current flowing in the R_p resistance, obtained by applying Kirchhoff's current law to the node.

Prelab

1. Simulate the circuits in Fig 6.4 and Fig 6.5 with the values mentioned below in the component list and write the results in Table 6.2 and Table 6.3.
2. Prepare a short report with simulation results.

Procedure

Electric Diagrams

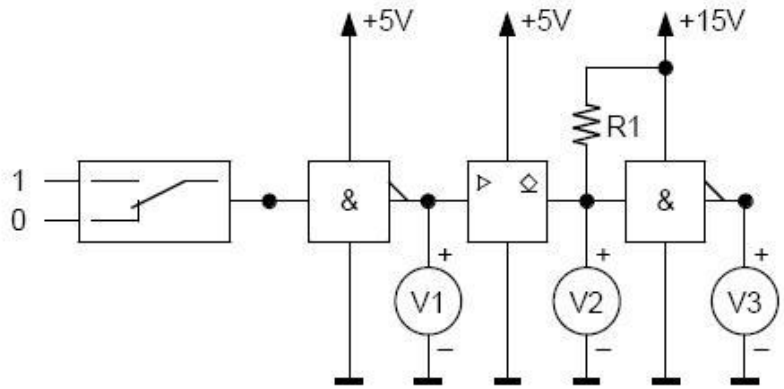


Fig 6.4

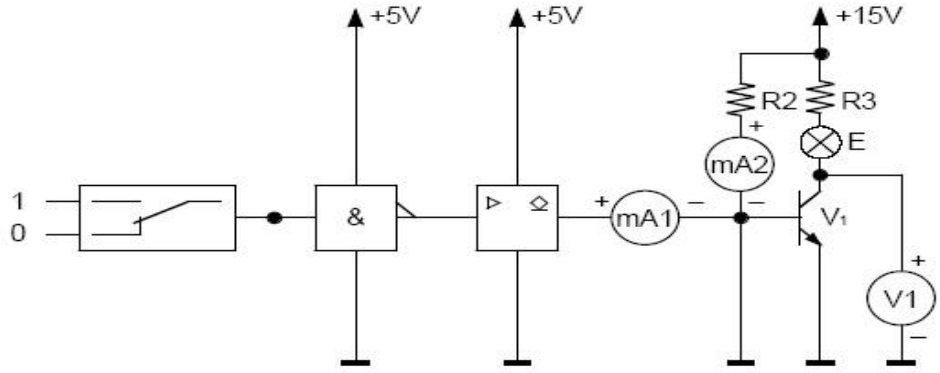


Fig 6.5

Components List

R1 = 3 kΩ , R2, R3 = 330 Ω, N1 = 74LS00 (TTL NAND gate) N2 = 7407 (open collector Hex buffer), N3 = 4011 (CMOS NAND gate),V1 = 2N1711 transistor.

Experiment

TTL TO CMOS INTERFACING

1. Insert Module 20 in the console and set the main switch to ON.
2. Connect the circuit and the voltmeters, as shown in Fig. 6.4.
3. Set the input to logic 0.
4. Read the meters indications and write them in Table 6.2.
5. Set the input to logic 1.
6. Read the meters indications and write them in Table 6.2.
7. Remove all the connections.

TTL TO ANY LOAD INTERFACING

1. Connect the circuit, the voltmeter and the ammeters as in Fig. 6.5.
2. Set the input to logic 0.
3. Read the meters indications and write them in Table 6.3.
4. Set the input to logic 1.
5. Read the meters indications and write them in Table 6.3.
6. Remove all the connections.

Results

V_I (V)	V_1 (V)	V_2 (V)	V_3 (V)
Logic 0			
Logic 1			

Table 6.2

V_I (V)	I_1 [mA]	I_2 [mA]	V_1 [V]
Logic 0			
Logic 1			

Table 6.3

German Jordanian University
School of Electrical Engineering and Information Technology
Digital Electronics Laboratory (ECE 5420)

Laboratory Experiment (7)

Comparator and Schmitt trigger

Objectives

To build a comparator and a Schmitt trigger using an operational amplifier O.A. and study their characteristics.

Instruments

DL 3155M16 module (unit #5), oscilloscope, signal generator, 2 digital multi-meters, cable set.

Theory

The comparator circuit compares an unknown signal voltage with a known threshold voltage to determine whether the signal is higher or lower than this threshold. When the threshold voltage is set to zero, the comparator can be used as a zero detector. When the signal is connected to the inverting input of the O.A and the threshold is set to zero as shown in Fig. 7.1, the circuit will be an inverting comparator and the output will be high when the input signal is negative. When the signal is connected to the noninverting input of the O.A and the threshold is set to zero as shown in Fig. 7.2, the circuit will be a noninverting comparator and the output will be high when the input signal is positive.

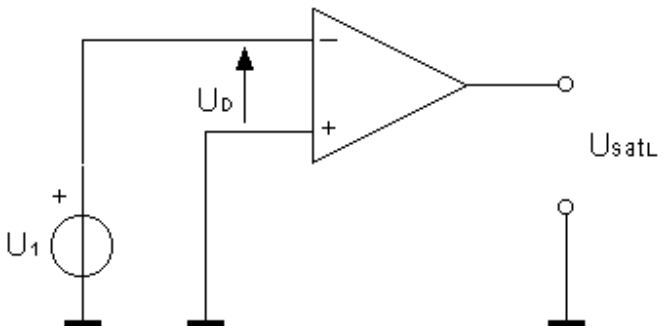


Fig. 7.1

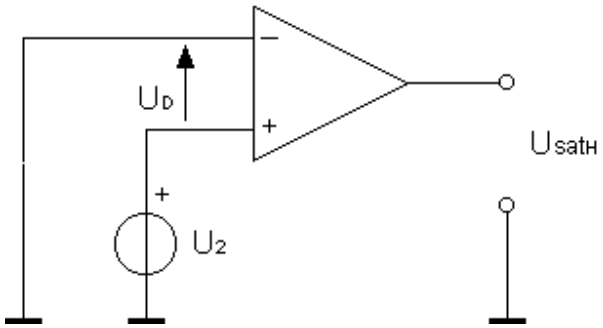


Fig. 7.2

If the input signal is a sinusoidal signal, then the output signal of the noninverting comparator will have a rectangular form as shown in Fig. 7.3. The output will be reversed in the case of an inverting comparator.

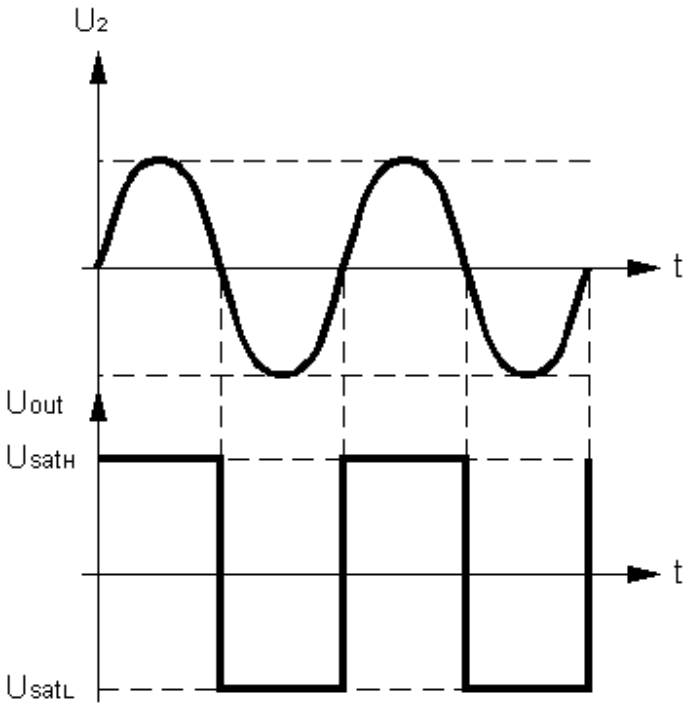


Fig. 7.3

Schmitt Trigger

We have observed in the comparator operation that if we apply to one of its inputs a reference voltage V_{ref}, the output swings between ±Vcc, as soon as the voltage of the other input goes through the threshold value V_{ref}, besides the comparator realized in this way has an instability area around the reference value.

Obviously, any disturbance (noise) near this threshold voltage can make the output state unpredictable. We can remove this instability by means of a positive feedback as shown in Fig. 7.4. However, this will give rise to a small HYSTERESIS around the reference value as shown in Fig. 7.5.

In this case, we will have two different threshold voltages U_{tH} and U_{tL} which are given by:

$$U_{tH} = \frac{R_1}{R_1 + R_2} \cdot U_{satH} \qquad U_{tL} = \frac{R_1}{R_1 + R_2} \cdot U_{satL}$$

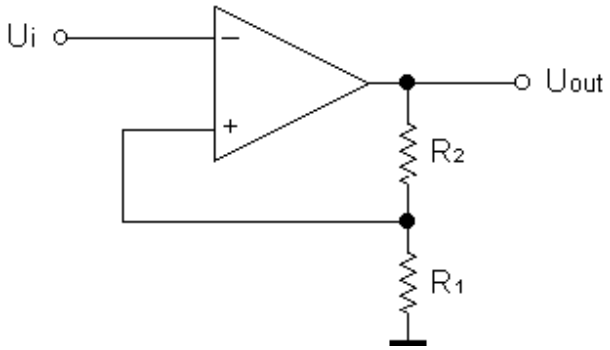


Fig. 7.4

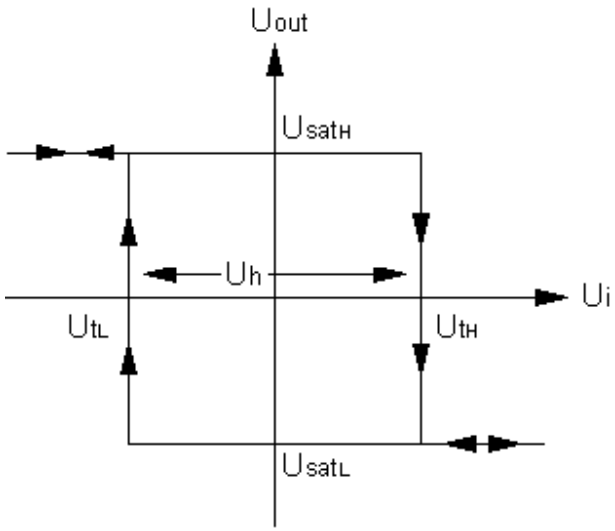


Fig. 7.5

The magnitude of the hysteresis U_h is given by:

$$U_h = U_{tH} - U_{tL} = \frac{R_1}{R_1 + R_2} (U_{satH} - U_{satL})$$

The interval $U_{satL} < U_i < U_{satH}$ is called DEAD AREA because the U_i variations in this area don't produce output variations. Besides, in this area, the output can be either high or low depending on the previous history of U_{out}. From the U_h expression, we can see that the hysteresis amplitude can be modified by varying the ratio R_1/R_2.

Prelab

1. Simulate all circuits from Fig 7.6 to Fig. 7.9 with the values mentioned below in the components list.
2. Prepare a short report with simulation results.

Procedure:

Electrical Diagrams

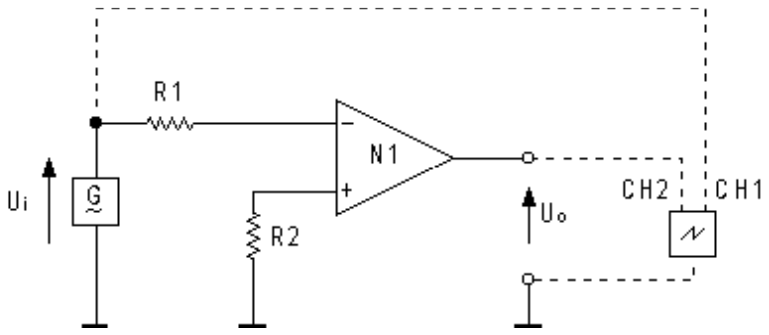


Fig. 7.6

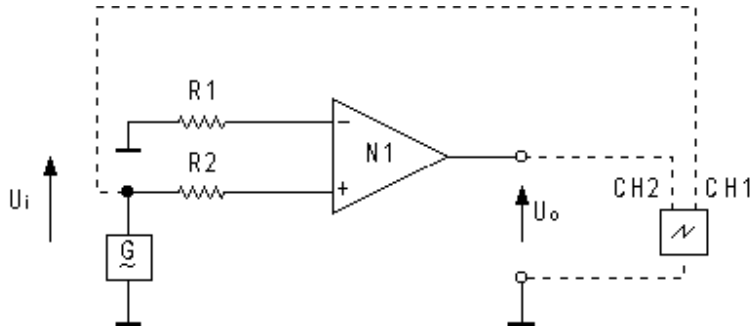
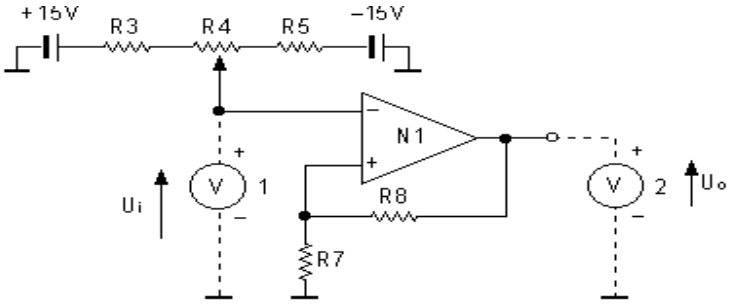


Fig. 7.7



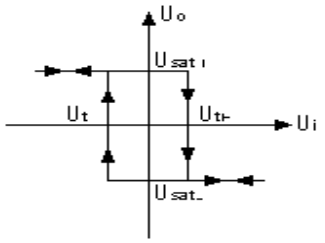


Fig. 7.8

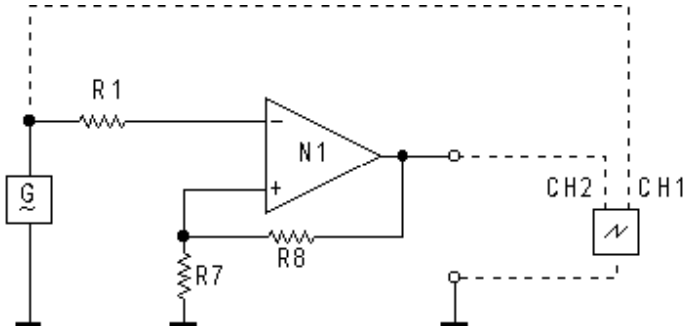


Fig. 7.9

Components List

R1 = 2.2 kΩ, R2 = 5 KΩ, R3 = 5.6 kΩ, R4 = 2.7 kΩ, R5 = 5.6 kΩ, R6 = 10 kΩ, R7 = 1 kΩ, R8 = 100 kΩ , N1 = µA741 (operational amplifier)

Calculation data

Inverting comparator:	if $U_i < U_{ref}$ -> $U_o = U_{satH}$ if $U_i > U_{ref}$ -> $U_o = U_{satL}$
Non inverting comparator:	if $U_i > U_{ref}$ -> $U_o = U_{satH}$ if $U_i < U_{ref}$ -> $U_o = U_{satL}$ U_{ref} = reference voltage U_{sat} = saturation voltage (H positive, L negative) $12V < U_{sat} < 15V$
Inverting comparator with hysteresis (Schmitt trigger):	U_{tH} = higher threshold voltage U_{tL} = lower threshold voltage U_h = hysteresis amplitude If $U_{tH} = - U_{tL}$ symmetrical hysteresis cycle, $U_h = U_{tH} - U_{tL}$ $U_{tH} = R7/(R7+R8) \cdot U_{satH}$ with S1 in OFF $U_{tL} = R7/(R7+R8) \cdot U_{satL}$ with S1 in OFF $U_{tH} = R6/(R6+R8) \cdot U_{satH}$ with S1 in ON $U_{tL} = R76(R6+R8) \cdot U_{satL}$ with S1 in ON

Experiment

INVERTING COMPARATOR

1. Insert Module 16 in the console and set the main switch to ON.
2. Connect the signal generator and the oscilloscope as shown in Fig. 7.6.
3. Adjust the oscilloscope in the following way:
   CH1 = 1 V/DIV,
   CH2 = 5 V/DIV
   TIME/DIV = 250 µs,
   coupling = AC;

4. Supply the signal generator and adjust the sinusoidal output signal to 4V peak-to-peak - 1KHz.
5. Observe, on the oscilloscope display, the output signal of the inverting comparator. This signal is a positive square wave when the input signal decreases and negative when the signal increases. In this case the voltage U_{ref} is equal to zero. Because of the very high gain of the open loop O.A., the output becomes immediately negative as soon as $U_i > U_{ref}$, and vice versa.

6. Draw the signals displayed on the oscilloscope by drawing with a dashed line the input wave and with a continuous line the output wave.

NON INVERTING COMPARATOR

1. Connect the circuit as shown in Fig. 7.7.
2. Repeat the previous operations (1-6) and describe the differences between the behavior of this circuit with the previous one.

SCHMITT TRIGGER

1. Connect the circuit shown in Fig.7.8.
2. Set the switch S1 to OFF and turn the potentiometer R_1 completely clockwise and check the comparator output. It should have the positive saturation voltage U_{satH}.
3. Turn slowly the potentiometer R_4 counterclockwise, until the threshold voltage value U_{tH} is surpassed so that, on the comparator output, there is the negative saturation voltage U_{satL}.
4. Write down the voltage values U_{tH}.
5. Turn slowly the potentiometer R_2 clockwise, until the threshold voltage value U_{tH} is surpassed so that, on the comparator output, there is the positive saturation voltage U_{satH}.
6. Write down the voltage values U_{tL}.
7. Calculate the negative and positive threshold voltages and write down their values.
8. Compare the measured values with the calculated ones.
9. Set the switch S1 to ON.
10. Repeat steps 3 to 8.
11. Connect the signal generator and the oscilloscope as shown in Fig. 7.9.
12. Adjust the oscilloscope in the following way:
    CH1 = 1V/DIV
    CH2 = 1V/DIV,
    TIME/DIV = 0.2ms,
    coupling = AC.

13. Supply the signal generator and adjust the function generator to generate sinusoidal output signal of 4 V peak-to-peak - 1KHz.
14. Observe, on the oscilloscope display, the output signal of the comparator. This signal is a square wave, inverted against the input signal, and its commutation doesn't happen in correspondence of the passage through zero of the input signal, as for the inverting comparator, but only when the value of the threshold voltages are reached.
15. Draw the signals displayed on the oscilloscope by drawing with a dashed line the input wave and with a continuous line the output wave.
16. Set the oscilloscope in the X-Y mode to display the transfer characteristics.
17. Draw the transfer characteristics.

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Digital Electronics Laboratory (ECE 5420)

Laboratory Experiment (8)

555 Timer as Monostable & Astable Multivibrators

Objectives

To show how a 555 Timer can be used as monostable and astable multivibrators.

Instruments

DL 3155M16 module (units # 8 & 9), Oscilloscope, Signal generator, and cable set.

Theory

The 555 timer is a component of a hybrid kind (digital and analog) and it is used as a square wave generator (Astable multivibrator) or as a timing circuit (Monostable multivibrator). It is available as an integrated circuit made up of a series of three equal resistances, two comparators, an R-S flip-flop, an inverting buffer, and a bipolar transistor as a switch as shown in Fig. 8.1. The three resistors are used as a voltage divider which gives threshold voltages for the two comparators. The first threshold voltage is equal to 2/3Vcc and it is connected to the inverting input of the first comparator. The second threshold voltage is equal to 1/3Vcc and it is connected to the noninverting input of the second comparator. The output of the 1^{st} comparator is connected to the reset input of the flip-flop and it resets the F.F. when it is high (S = 0, R = 1 $\Rightarrow$ Q = 0) or when the limit (threshold) voltage is higher than 2/3Vcc. The output of the 2^{nd} comparator is connected to the set input of the flip-flop and it sets the F.F. when it is high (S = 1, R = 0 $\Rightarrow$ Q = 1) or when the trigger voltage is less than 1/3Vcc. When the F.F. is in the set state, the transistor is open, otherwise it is closed. The output of the inverting buffer is high when the F.F. is in the set state. The F.F. can be reset externally by applying a low voltage to the external reset pin. The pin diagram for the 555 integrated circuit is shown in Fig. 8.2.

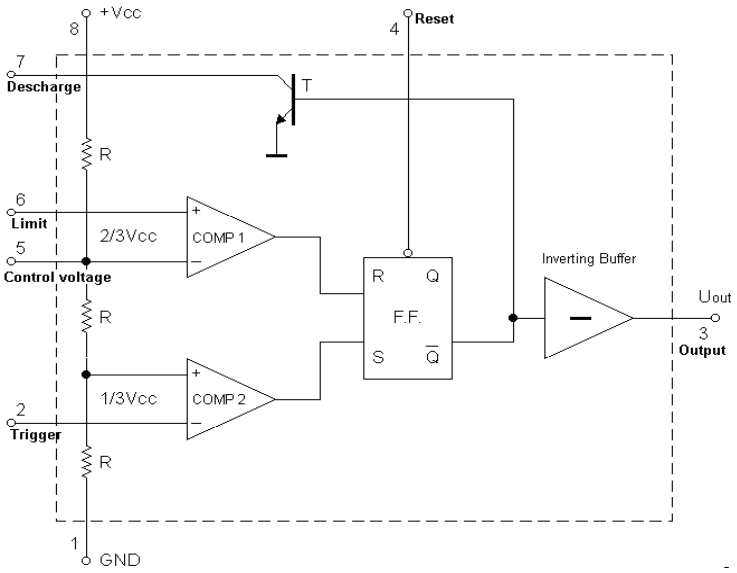

Fig. 8.1

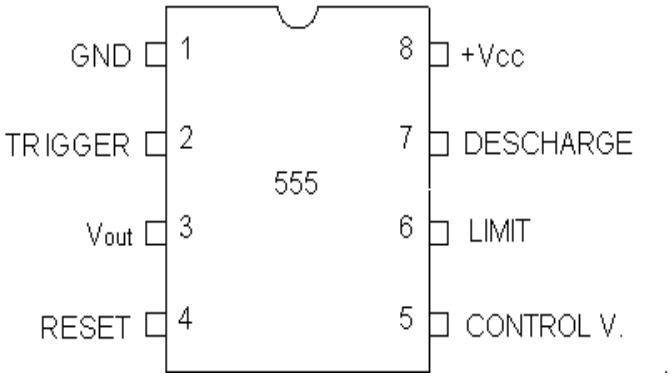

Fig. 8.2

555 timer as astable multivibrator

The connection of the 555 timer as astable multivibrator is shown in Fig. 8.3. Both the limit and the trigger voltages depend on the voltage across the external capacitor C. If the voltage across the capacitor is less than 1/3Vcc, the F.F. is set and the transistor is open and the capacitor starts to charge from V_{CC} through $R_1 + R_2$. If the voltage across the capacitor exceeds 2/3Vcc, the F.F. is reset ant the transistor is closed and the capacitor discharges into the transistor through R_2. The cycle will be repeated continuously as shown in Fig. 8.4 where the capacitor charges from 1/3Vcc to 2/3Vcc with a time constant $\tau_1 = (R_1 + R_2)\, C$ and the output is high, and it discharges from 2/3Vcc to 1/3Vcc with a time constant $\tau_2 = R_2\, C$ and the output is low. The cycle consists of two intervals: the charge time which is equal to $T1 = (R_1 + R_2)\, C \ln (2)$ and the discharge time which is equal to T2 = R2 C ln (2).

The square wave period is equal to $T = (R_1 + 2 \cdot R_2) C \ln(2)$ and its frequency is equal to $f = 1 / T = 1/ [(R_1 + 2 R_2) C \ln 2]$ and the duty cycle (D.C.) is equal to $D.C. = T_1 / (T_1 + T_2) = (R_1 + R_2) / (R_1 + 2 R_2) > 0.5$.

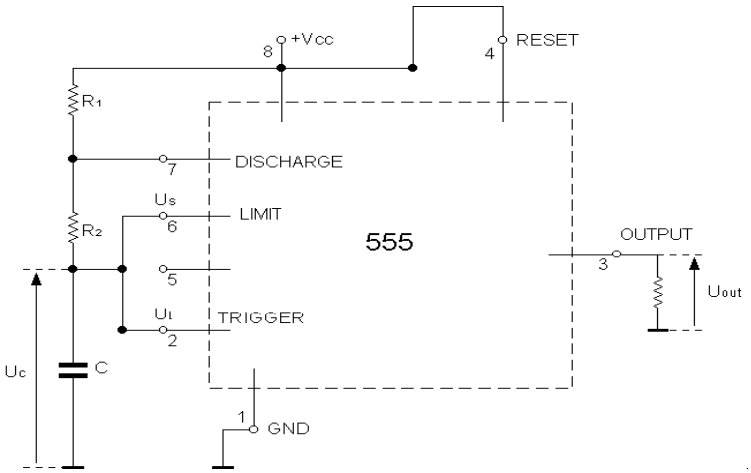

Fig. 8.3

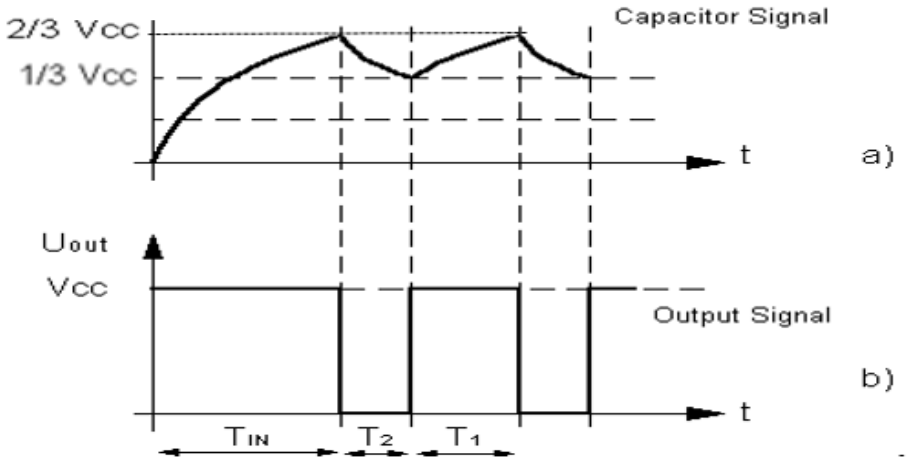

Fig. 8.4

555 timer as a monostable multivibrator

The monostable gives a pulse with a specified width at its output when it is triggered by the edge of an external input pulse. The connection of the 555 timer as a monostable multivibrator is shown in Fig. 8.5. Both the limit and the discharge pins are connected across the external capacitor C. When the voltage of the trigger is higher than 1/3Vcc, the F.F. is in the reset state and therefore the transistor is closed and the capacitor voltage will be zero and the output is low. The 555 timer remains in this stable state as long as the trigger voltage is high. When the voltage of the trigger goes below 1/3Vcc for a very short time, the output of comparator 2 becomes high and the F.F. will be set and therefore the transistor will be open and the capacitor starts to charge toward V_{CC} with a time constant $\tau = R_1 C$ as shown in Fig. 8.6. In this period, the output of the inverting buffer is high. When the voltage of the capacitor exceeds 2/3Vcc, the output of comparator 2 becomes high and the F.F. will be reset and therefore the transistor will be closed and the capacitor discharges instantly to zero and the output will be low again. The duration of the output pulse can be easily derived and it is given by: $T = R_1 C \ln(3) = 1.1 R_1 C$

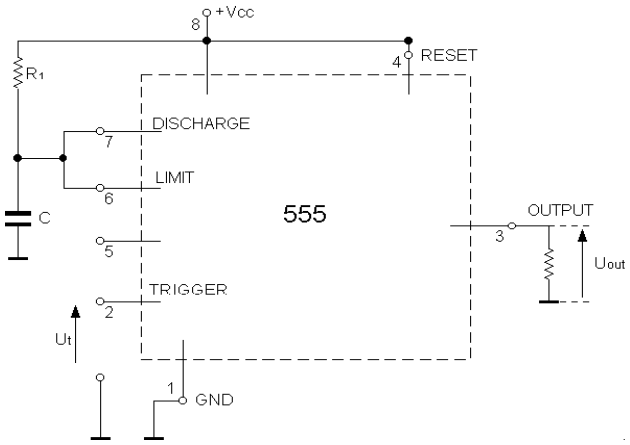

Fig. 8 .5

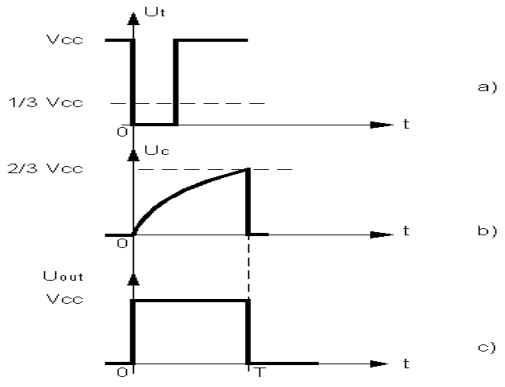

Fig. 8.6

Prelab

1. Simulate the circuits in Fig 8.7 and Fig 8.8 with the values mentioned below in the components list and write the results in Table 8.1.
2. Prepare a short report with simulation results.

Procedure

555 as astable multivibrator

Electrical Diagrams

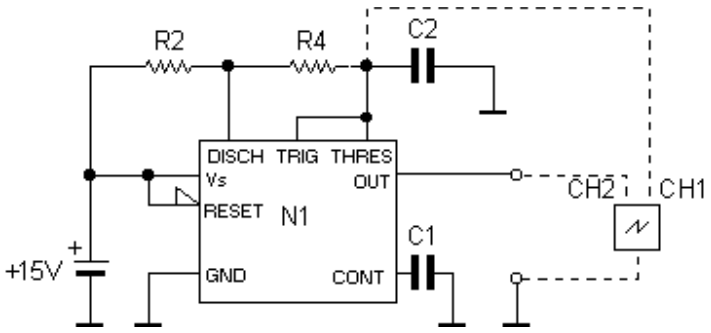

Fig. 8.7

Components List

R1 = 100 KΩ, R2 = 10 KΩ, R3 = 10 KΩ, R4 = 100 KΩ, C1 = 22µF - 50V – Polyester, = 10µF - 50V – Polyester, C3 = 10µF - 50V – Polyester, N1 = 555

Calculation data

Output frequency: $f = \frac{1.443}{(R2 + 2 \cdot R4) \cdot C2}$ [Hz] with S1, S2 and S3 OFF

Duty cycle % : $dc\% = \frac{R2 + R4}{R2 + 2 \cdot R4} \cdot 100$ with S1, S2 and S3 OFF

Results

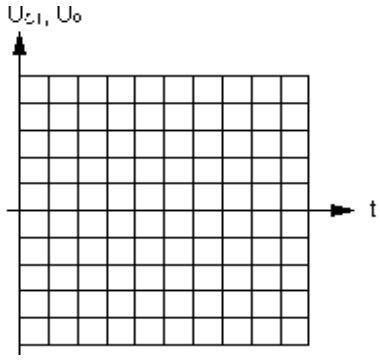

Fig. 8.8

	U_0 [V]	t_1 [sec]	t_2 [sec]	f [Hz] measured	f [Hz] calculated	Duty cycle % measured	Duty cycle % calculated
S1,S2,S3 = OFF (R2,R4,C2)							
S1,S2 = ON S3 = OFF (R1,R3,C2)							
S1= ON S2, S3 = OFF (R1,R4,C2)							
S1,S2 = OFF S3 = ON (R2,R4,C3)							

Table 8.1

Experiment

1. Insert Module 16 in the console and set the main switch to ON;

MEASURE OF THE PULSE AMPLITUDE

2. Connect the signal generator and the oscilloscope as shown in Fig. 8.7.
3. Adjust the oscilloscope in the following way: CH1 = 5V/DIV, CH2 = 5V/DIV, TIME/DIV = 0.5ms, coupling = DC.
4. Set the switches S1, S2 and S3 to OFF;
5. Measure the pulse amplitude and write the value in Table 8.1.

MEASURE OF THE PULSE DURATION

6. Measure the half-period t_1 and t_2 and write the values in Table 8.1.

MEASURE OF THE PULSE FREQUENCY

7. Measure the frequency and write the value in Table 8.1.
8. Calculate the frequency value, write it in Table 8.1 and compare it with the measured one.
9. Draw the signal at the capacitor C_1 ends (jack 2) in Fig. 8.7, together with the output signal.

MEASURE OF THE DUTY CYCLE

10. Determine the percent duty cycle of the output signal and write the result in Table 8.1.
11. Calculate the duty cycle with the formula written in "calculation data" and compare the result with the one obtained with the previous formula.
12. Repeat the previous operations by moving the switches S1, S2 and S3 as shown in Table 8.1 and describe the differences that have been found.

555 as a monostable multivibrator

Electrical Diagrams

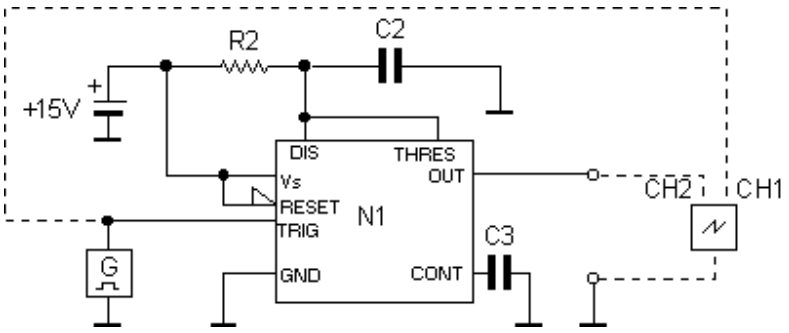

Fig. 8.8

Components List

R1 = 33 kΩ, R2 = 47 kΩ, C1 = 0.1 µF -50V – Polyester, C2 = 0.01 µF – 50 V – Polyester, C3 = 0.01 µF – 50 V – Polyester N1 = 555

Calculation data

$t_1 = 1.1\ R2 \cdot C2$ with S1, S2 Y S3 OFF

Results

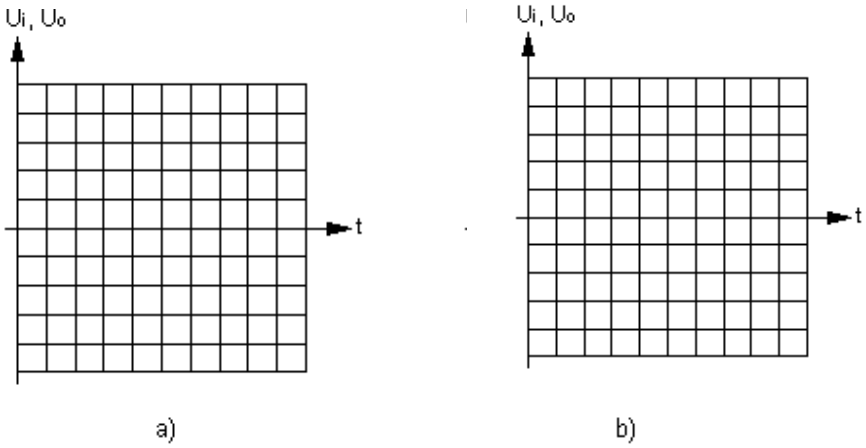

Fig. 8.10

	t_1 [sec] measured	t_1 [sec] calculated
S1, S2 = OFF		
S1, S2 = ON		

Table 8.2

1. Insert Module 16 in the console and set the main switch to ON.
2. Connect the circuit as shown in Fig. 8.8.
3. Note: *the switches of the astable multivibrator have to be set in the following way: S1, S2, S3 to ON.*
4. adjust the oscilloscope in the following way:
   CH1 = 5V/DIV;
   CH2 = 5V/DIV,
   TIME/DIV = 1ms;
   Coupling = DC;

5. Observe, on the oscilloscope display, the input and output signals and draw them in Fig. 8.10-a.
6. Measure the output pulse width and write the value in Table 8.2.
7. Calculate the output pulse width and write the value in Table 8.2.
8. Repeat the previous operations by moving, in the same time, the switches S1, S3 to ON, S2 to OFF of the astable multivibrator and the switches S1 and S2 of the monostable multivibrator to ON and draw in Fig. 8.10-b the signals displayed on the oscilloscope display.

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Laboratory Experiment (9)

Square wave and Ramp Generators

Objectives

The objective of this experiment is to build a square wave and ramp generators using operation of amplifiers (O.A.).

Instruments

DL 3155M16 module (units # 6 & 7), Oscilloscope, Signal generator, and cable set.

Theory

Part 1: Square Wave Generator

The square wave generator is an astable multivibrator circuit whose output oscillates continuously between two prefixed states, giving therefore a square or rectangular wave, whose period depends on the circuit time constants. The square wave generator is an O.A. with two feedback mechanisms as shown in Fig. 9.1; a negative one (made up of the resistor R_f and the capacitor C) that determines the time constant by which the capacitor is charged and gives the voltage U_2, and a positive one (made up of the divider R_1 and R_2) that gives the threshold voltage to the noninverting terminal (U_1) which is given by:

$$U_1 = \frac{R_2}{R_1 + R_2} U_{out} = \beta \cdot U_{out}$$

where U_{out} can assume only the two values U_{satH} and U_{satL}

Let's suppose at the beginning that $U_{out} = U_{satH} \Rightarrow U_1 = \beta \cdot U_{satH} = U_{tH}$, in this case the capacitor C starts to charge towards the value U_{satH} with time constant $\tau = R_f \cdot C$. But, when U_2 exceeds the threshold value U_{tH} (upper threshold voltage) at instant t_1, the output U_{out} switches abruptly to its low level U_{satL}, and the voltage U_1 becomes:

$$U_1 = \beta \cdot U_{satL} = U_{tL}$$

The capacitor now starts to discharge towards the value U_{satL} ($t_1 < t < t_2$) until it reaches $U_1 = U_{tL}$ (U_{tL} lower threshold voltage), at instant t_2 and at this point the output changes its state again moving to the value U_{satH} and the cycle is repeated as shown in Fig. 9.2. We have from Fig. 9-2 (assume $U_{satH} = -U_{satL}$):

$$T_1 = T_2 = \tau \cdot \ln \frac{1+\beta}{1-\beta} \qquad \tau = R_f \cdot C$$

$$T = T_1 + T_2 = \frac{1+\beta}{1-\beta} = 2 \cdot \tau \cdot \ln \left(1 + \frac{2 \cdot R_2}{R_1}\right)$$

$$f = \frac{1}{T} = \frac{1}{2 \cdot \tau \cdot \ln (1 + 2R_2/R_1)}$$

The assumption that $U_{satH} = -U_{satL}$ is necessary to obtain a square wave with the same positive and negative values.

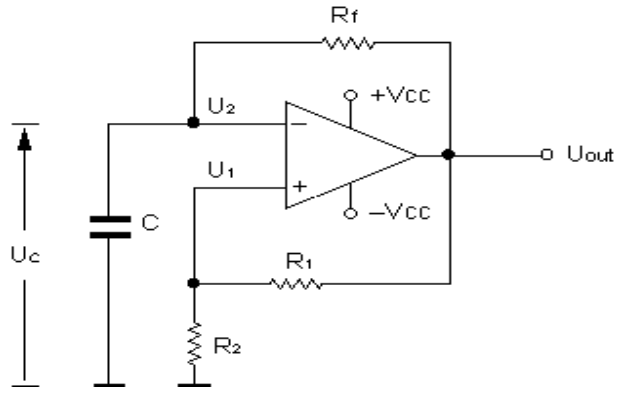


Fig. 9.1

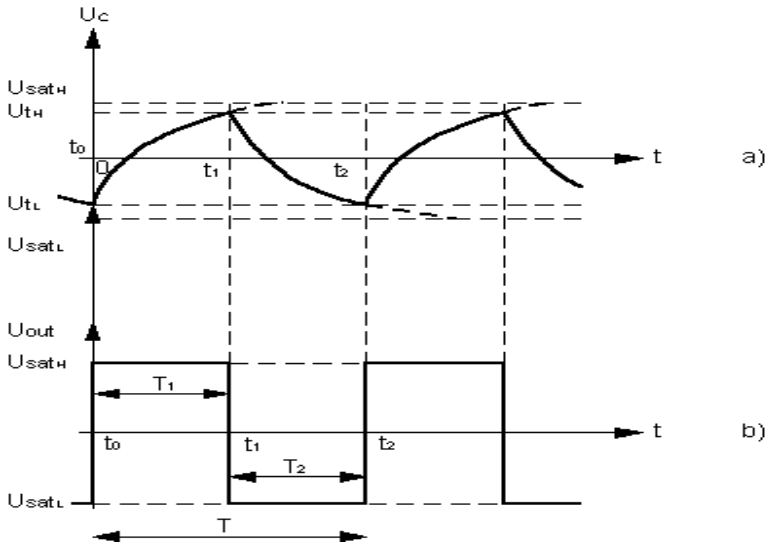


Fig. 9.2

Part 2: Ramp Generator

A ramp or saw-tooth signal can be generated by charging a capacitor by a constant current source and then discharging it quickly. The input signal U_{in} is a sinusoidal signal with a specified amplitude and a frequency which determines the frequency of the ramp generator. The ramp generator circuit is shown in Fig. 9.3. The first O.A. (N1), compares the input signal U_{in} with the output signal U_{out} of the second O.A.(N_2) and its output voltage U'_{out} will swing between two values which is limited by the two Zener diodes V_1 and V_2. The second O.A. (N2), integrates the output signal of the first O.A. which can be adjusted using the potentiometer R_2. If $U_{out} = U_{in} \Rightarrow U_{out} = 0$ and the output voltage U_{out} remains constant to the desired value. If $U_{in} > U_{out} \Rightarrow U'_{out} < 0$: the diode V_4 will conduct since it is forward biased, while diode V_3 is off since it is inverse biased. Now the current in diode V_4 is a constant current and its value is determined by dividing the voltage supplied by the potentiometer R_2 minus the drop across the diode by R_5 since its other end is connected to the virtual ground. Now the capacitor C starts to charge linearly by this constant current giving a positive saw-tooth waveform. The slope of this saw-tooth or ramp signal can be varied by the potentiometer R_2. When U_{out} exceeds U_i, the output of O.A. changes to the positive value and since $U_{in} < U_{out} \Rightarrow U'_{out} > 0$. In this case, the diode V_4 doesn't conduct while the diode V_3 conducts and the capacitor starts to discharge through V_3 and R_4. If R_4 is chosen to be very small compared with R_5 , the capacitor will discharge very quickly. The frequency of the ramp generator is the same as the frequency of the input signal but its amplitude and slope are controlled by the potentiometer R_2, the resistor R_5 and the capacitor C_1.

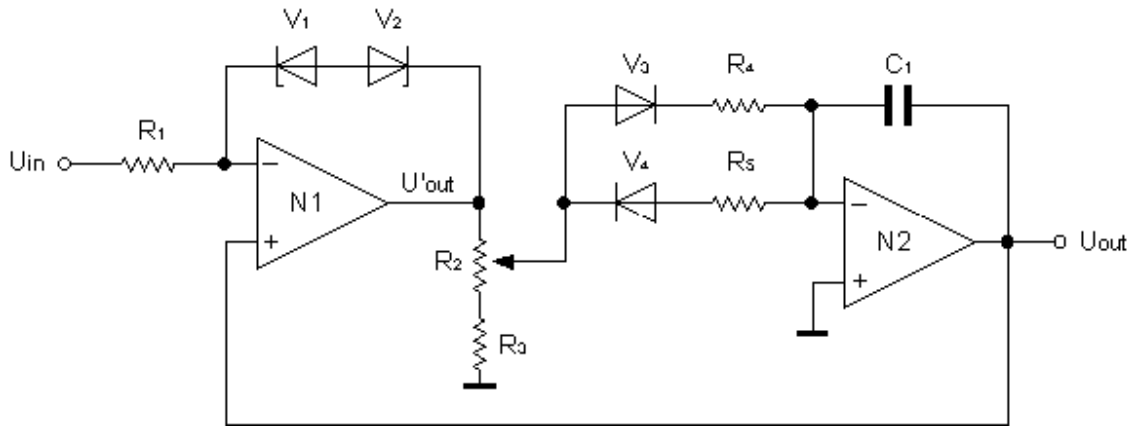


Fig. 9.3

Prelab

1. Simulate the circuits in Fig 9.4 and Fig 9.6 with the values mentioned below in the components list and write the results in Table 9.1 and Table 9.2.
2. Prepare a short report with simulation results.

Procedure

Part 1: O.A. as a square generator

Electrical Diagrams

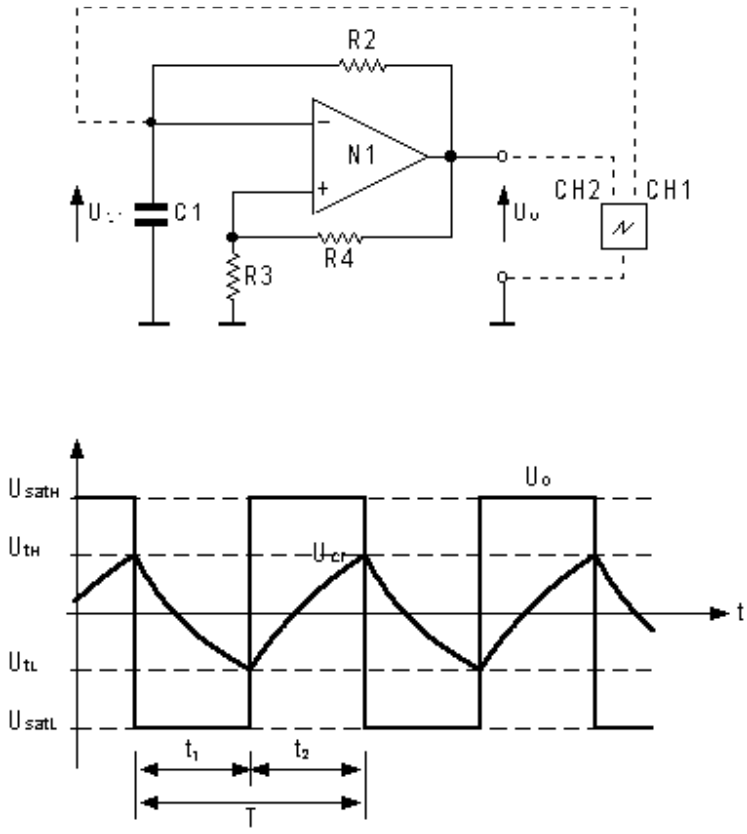


Fig. 9.4

Components List

R1 = 56 kΩ, R2 = 10 kΩ, R3 = 10 kΩ, R4 = 10 kΩ, C1 = 0.047 µF - 50V – Polyester; C2 = 0.1 µF -50 V – Polyester; N1 = µA741.

Calculation data

Frequency measurement:

$$f_t = \frac{1}{t_1 + t_2} = \frac{1}{T} \quad [Hz]$$

$$f_t = \frac{1}{2 \cdot R2 \cdot C1 \cdot \ln[1 + (2 \cdot R3 / R4)]} \quad [Hz] \text{ with S1 and S2 in OFF}$$

Obtained Results

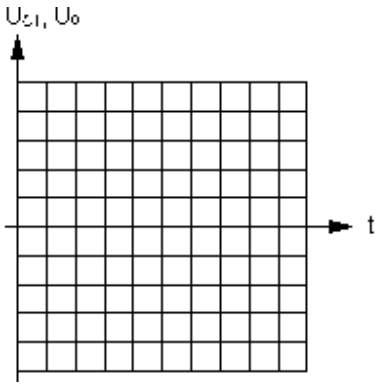


Fig.9.5

	t_1 [sec]	t_2 [sec]	T [sec]	f [Hz] measured	f [Hz] calculated
S1 = OFF, S2 = OFF					
S1 = ON, S2 = OFF					
S1 = OFF, S2 = ON					
S1 = ON, S2 = ON					

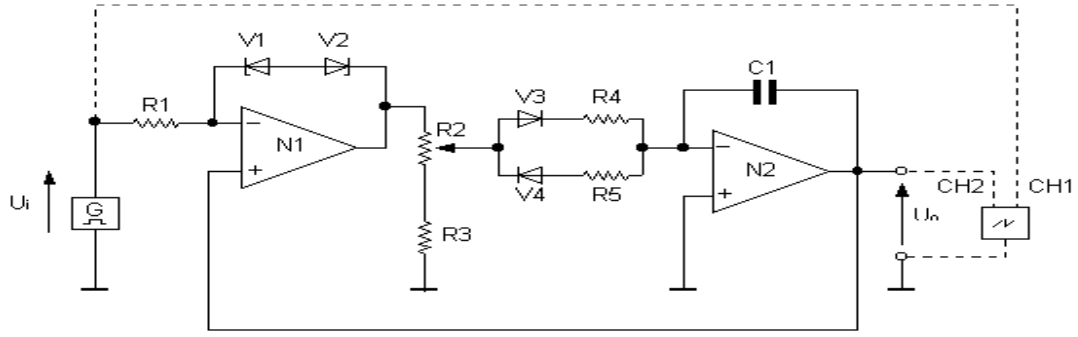
Table 9.1

Experiment

1. Insert Module 16 in the console and set the main switch to ON.
2. Connect the signal generator and the oscilloscope as shown in Fig. 9.4.
3. Adjust the oscilloscope in the following way:
   CH1 = 5V/DIV
   CH2 = 5V/DIV,
   TIME/DIV = 0.2ms,
   coupling = DC;
4. Set the switches S1 and S2 to OFF.
5. Measure the half-period t_1 and t_2 and write the values in Table. 9.1.
6. Measure the frequency and write the value in Table. 9.1.
7. Calculate the frequency value, write it in Table 9.1 and compare it with the measured one.
8. Draw the signal at the capacitor C_1 ends (jack 1) in Fig. 9.5 along with the output signal.
9. Repeat the previous operations by moving the switches S1 and S2 according to Table 9.1 and observe what happens.

Part 2: Ramp Generator

Electrical Diagrams



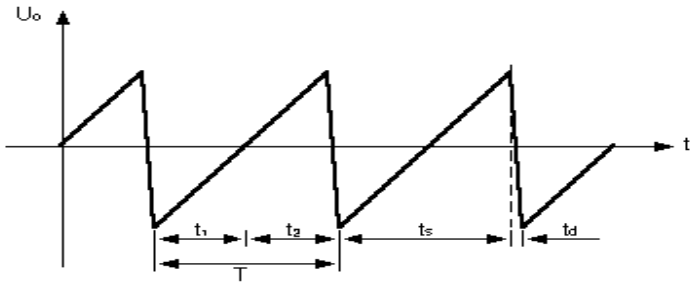


Fig.9.6

Components List

R1 = 10 kΩ, R2 = 10 kΩ, R3 = 470 Ω, R4 = 330 Ω, R5 = 10 kΩ, C1 = 0.1 µF – 50 V ;Polyester; V1 = Zener diode – 10 V - 0,5 W; V2 = Zener diode – 10 V - 0,5 W; V3 = 1N4148; V4 = 1N4148; N1 = µA741; N2 = µA741

Calculation data

Frequency measurement:

$$f = \frac{1}{t_1 + t_2} = \frac{1}{T} \text{ [Hz]}$$

Results

t_1 [sec]	t_2 [sec]	f [Hz]

Table 9.2

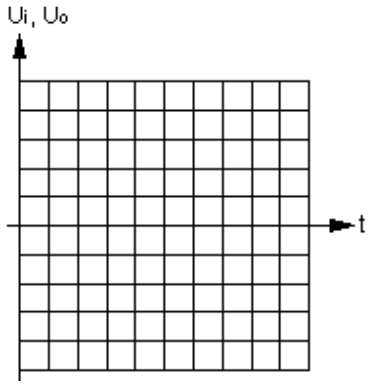


Fig. 9.7

Experiment

1. Insert Module 16 in the console and set the main switch to ON.
2. Connect the signal generator and the oscilloscope as shown in Fig. 9.6.
3. Adjust the oscilloscope in the following way:
   CH1 = 1V/DIV,
   CH2 = 0.5V/DIV
   TIME/DIV = 100 µs,
   coupling = AC;
4. Turn the potentiometer R2 completely clockwise.
5. Supply the signal generator and adjust the sinusoidal output signal to 4V peak-to-peak and 1- KHz.

6. Draw the ramp generator output signal shown on the oscilloscope display in Fig. 9.7.
7. Measure the half-period t1 and t2 and write the values in Table. 9.2.
8. Measure the frequency and write the value in Table 9.2.

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