German Jordanian University
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Communication Circuit Lab Manual

Experiment 7

Phased Locked Loop (PLL)

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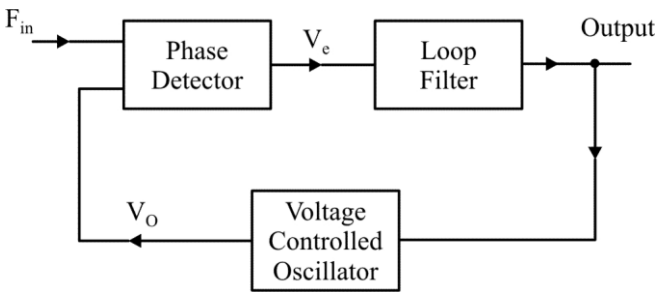
Theory

The phase-locked loop, or PLL, is one of the most useful blocks in modern electronic circuits. It is used for many different applications, ranging from communications (FM modulation, demodulation, frequency synthesis, signal correlation), control systems (motor control, tracking controls, etc), as well as applications such as pulse recovery and frequency multiplication.

A PLL is a closed-loop system, whose "purpose" is to lock an oscillator onto a provided input frequency (sometimes called the *reference frequency*) by "closed-loop," we mean that there is feedback from output to input. In a PLL, the feedback is negative, meaning that the system is self-correcting. Figure 1 shows the basic building blocks of a PLL.



Basic Phase locked Loop
Figure 1

This system consist of,

Phase Detector / Comparator:

When an input signal is applied to any PLL circuit, the phase comparator compares phase and frequency of this input signal with the phase and frequency of the VCO free running frequency and outputs a pulsating-DC waveform with a duty-cycle proportional to the phase difference ("error") between the two signals. The bigger the phase difference becomes (within certain limits, of course), the larger the duty cycle of the phase comparator's output becomes. If the two signals differ in phase and/or frequency, an error voltage is generated.

Voltage Controlled Oscillator:

A PLL has a special oscillator called a VCO, or Voltage Controlled Oscillator. The output frequency of the VCO is directly proportional to the error voltage that is actually the output of phase comparator. Any deviation in the frequency and/or phase of the two input signals to the phase comparator will generator error voltage which is further converted to the deviation in free running frequency of the VCO. In short, the VCO in effect converts the control *voltage* into *frequency*. The PLL under normal conditions attempts to make the VCO output frequency exactly equal to a second frequency that is applied to the PLL, the *reference frequency.*

Loop Filter:

The output of the phase comparator is a pulsating DC with a varying duty cycle. But the VCO needs a nice, steady DC voltage at its control voltage input. Also phase comparator output contains higher frequency components which can disturb the tuning of VCO as well as useless for VCO. In order to ensure this, the pulsating DC from the phase comparator is fed into a *loop filter* on its way to the VCO. This filter in effect "smoother" the rough phase comparator output waveform into a fairly steady DC voltage and also rejects the un-necessary frequency components present. The VCO will then be able to smoothly track the input reference frequency.

Phase Locked Loop Operation:

Let an input signal of frequency Fs is applied to the PLL. The other input (F_o) to the phase comparator comes from VCO output. The phase comparator compares the frequency and/or phases of the two signals and produces the sum (F_s+F_o) and difference (F_s-F_o) components at the output. The high frequency component (F_s+F_o) is removed by the loop filter and only the difference frequency component is amplified and applied to the VCO input. The V_e (error voltage) shifts the VCO frequency in the direction to reduce the frequency difference between Fs and F_o. Once the action started, the PLL is said to be in the capture range. The VCO continues to change the frequency till its output frequency is exactly equal to exactly equal to the input signal frequency. When such condition is achieved the PLL is said to be in locked. Once locked the PLL tracks the frequency changes in the input signal. Thus PLL undergoes three operating states. These are the *free-running*, *capture*, and *locked* states.

1. Free-running state:

The state when no reference input frequency being provided to the PLL. Design constants within the system determine what frequency the VCO.

2. Capture Range:

The range of frequencies over which the PLL can acquire lock with an input signal. This parameter is also expressed as the percentage of fo. The width of the capture range is determined by PLL design; the loop Low-Pass Filter is important in determining this.

3. Lock-in Range:

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the Lock-in range the lock range is usually expressed as the percentage of f_o. The lock range is less than or at the most equal to the capture range.

Figure 2 illustrates the relationship between free-running frequency, capture range, and lock range.

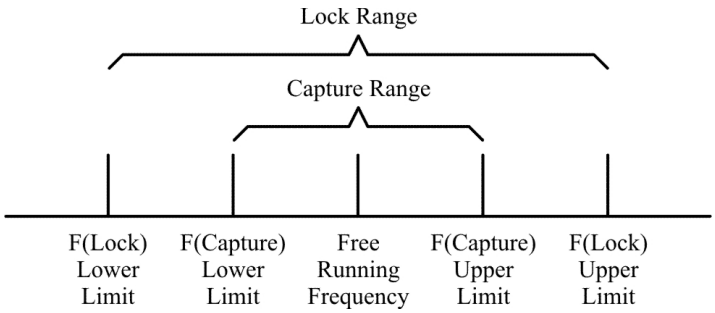


Figure 2

PLL as Frequency Multiplier/Divider:

The figure 3 shows the block diagram of PLL as frequency multiplier. A divide by N counter is inserted between the VCO output and phase comparator input. In locked state VCO output frequency is given by,

$$F_o = N * Fs$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

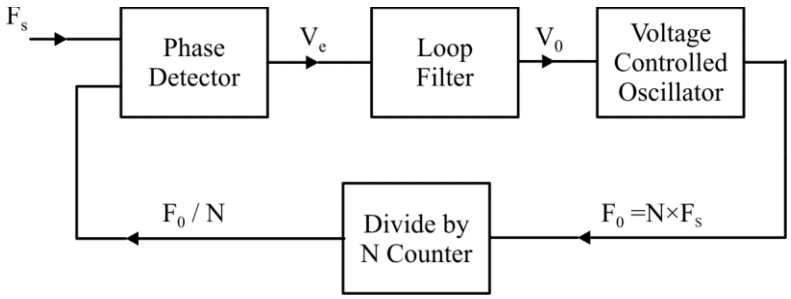


Figure 3

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the n^{th} harmonic of the input signal without connecting any frequency divider in between. However, as amplitude of the higher order harmonics becomes less, effective locking may not take place for high value of *n*. typically, *n* is kept less than 10.

The circuit in figure 4 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m^{th} harmonic of the VCO output with the input signal Fs. The output F_o of VCO is now given by,

$$F_o = Fs / m$$

Part 1

Objective:

Study of operation of Phase Locked Loop and Voltage Controlled Oscillator.

Equipments Needed:

1. Analog Board **AB25**.
2. DC power supplies +12V and -12V from external source or **Scientech 2612** Analog Lab.
3. Oscilloscope.
4. Function Generator.
5. Voltmeter.
6. 2mm Patch cords.

Circuit diagram:

Circuit used to study operation Phase Locked Loop is as shown in figure 4

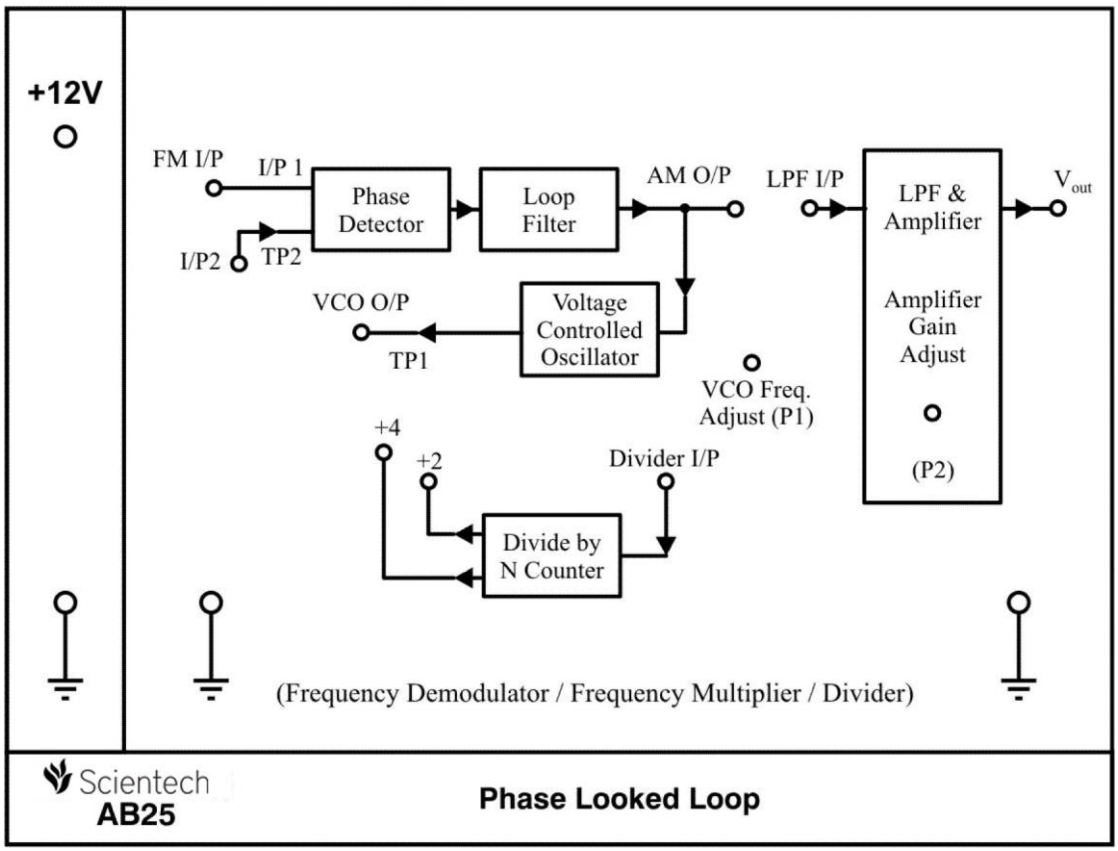


Figure 4

Procedure:

- Connect +12V and -12V DC power supplies at their indicated positions on **AB25** Board from external source or **Scientech 2612** Analog Lab.

1. Connect a 2mm patch cord between VCO output and phase comparator input (2).
2. Connect TP1 to Oscilloscope CH II and set VCO free-running frequency to 50 KHz.
3. Apply a sine wave signal (5 KHz freq. and 2Vp-p amplitude) from function generator or **Scientech 2612** Analog Lab at input (1) of phase comparator and observe the same signal on oscilloscope CH.I (put oscilloscope in dual mode).
4. Slowly increase the input frequency and observe VCO frequency variation w.r.t. the input signal frequency variation.
5. Keep on increasing input signal frequency up to the point when VCO frequency starts following the input frequency. Note down the frequency at which the process starts. This frequency is the lower capture frequency of the PLL.
6. Keep increasing the signal frequency further. A frequency is obtained when the VCO frequency stops following the input signal frequency. This frequency is the upper lock-in frequency. Observe that above the upper lock-in frequency the VCO signal will not at all follow the input frequency variation.
7. Now start reducing the input frequency slowly up to the value when again the VCO frequency starts following the input frequency. This frequency is upper capture frequency.
8. Keep reducing the signal frequency further to the value when VCO frequency stops following the input signal frequency and will not follow further. This value of the frequency is lower lock-in frequency.
9. Connect Digital Voltmeter at loop filter output i.e. at the output point named AM O/P and observe the variations of voltage for lock range. This also explains the operation of VCO.

   Phase comparator generates the error voltage (which can be observed on voltmeter). This voltage is fed to VCO which adjusts its output frequency according to the DC voltage at input.

10. Follow the above procedure when VCO free running frequency is

    a. 35 KHz.

    b. 65 KHz

Results:

- Free-running Frequency = ……..Hz
- Lower Capture Frequency = …….Hz
- Upper Capture Frequency = ……..Hz
- Lower Lock-in Frequency = ……..Hz
- Upper Lock-in Frequency = ……...Hz
- Capture Range ($F_{(Higher\text{-}cap)}$ - $F_{(Lower\text{-}cap)}$) =……Hz
- Lock-in Range($F_{(Higher\text{-}Lock)}$ - $Ff_{(Lower\text{-}Lock)}$) = ……Hz

Part 2

Objective:

Study of the operation of Phase Locked Loop as FM Demodulator

Equipments Needed:

1. Analog Board **AB25**.
2. DC power supplies +12V and -12V from external source or **Scientech 2612** Analog Lab.
3. Oscilloscope.
4. Function Generator
5. 2mm Patch cords.

Circuit diagram:

Circuit used to study operation of Phase Locked Loop as FM Demodulator is as shown in figure 4

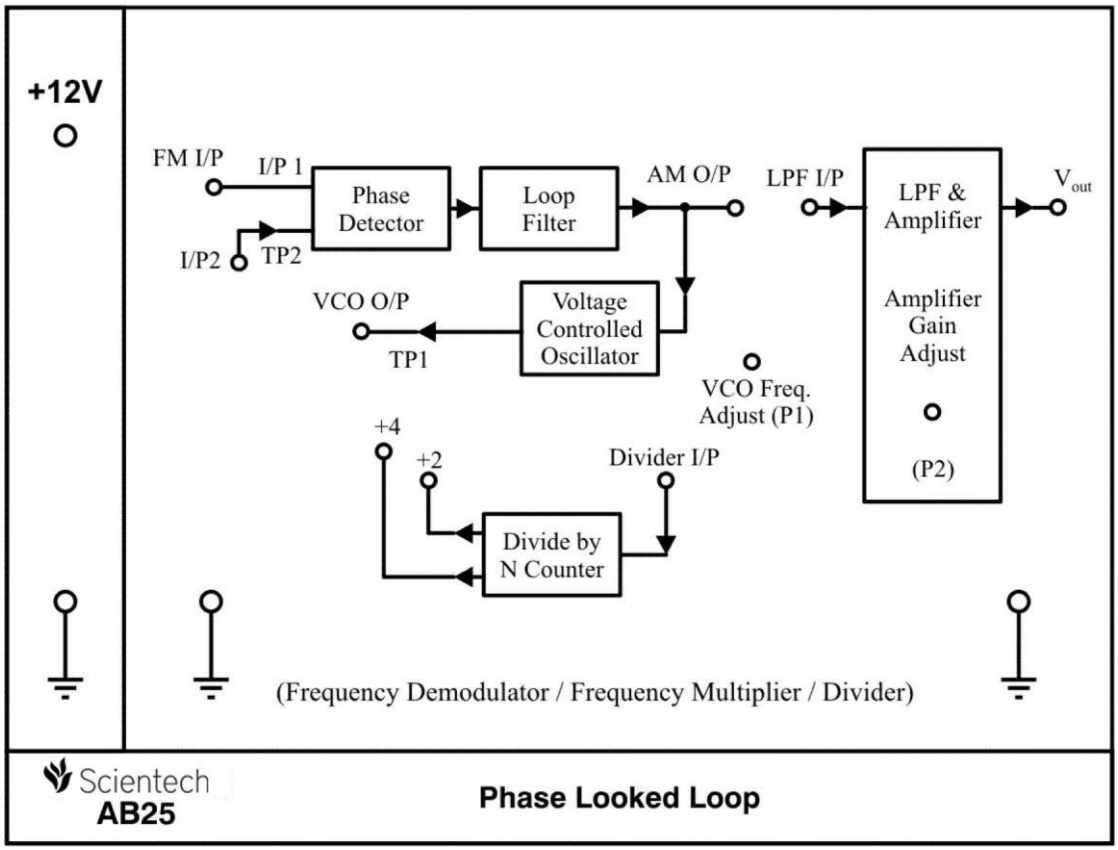


Figure 5

Procedure:

- Connect +12V and -12V DC power supplies at their indicated positions on **AB25** Board from external source or **Scientech 2612** Analog Lab.

1. Connect a 2mm patch cord between VCO output and phase comparator input (2).

2. Set VCO free-running frequency to 50 KHz by varying the VCO free running frequency pot and observing the same signal at test point TP1 on oscilloscope.

3. Apply a frequency modulated output signal from Function Generator (**Scientech 4063**) with carrier frequency 50 KHz amplitude 2Vpp and modulating signal amplitude 2Vpp frequency between 1 KHz to 3.3 KHz. Observe the modulating signal on CHI of oscilloscope.

4. Connect output of loop filter (AM output) to the input of LPF on **AB25** Board using a 2mm patch cord.

5. Observe the demodulated output between V_{out} (LPF & Amplifier output) and ground. If demodulated signal is not properly obtained then vary the VCO frequency adjust pot to obtain a pure modulating signal at output.

6. For obtaining output signal amplitude exactly equal to the modulating signal, vary the amplifier gain adjustment pot.